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Phase Disposition PWM Technique for Eleven Level Cascaded Multilevel Inverter with Reduced Number of Carriers

G. Sridhar[1] P. Satish Kumar[2] M. Sushama[3]

Abstract– Applying pulse width modulation (PWM) techniques for cascaded multilevel inverters are very complex for topologies with reduced number of switches. In this paper phase disposition (PD) pulse width modulation technique is implemented with lesser carrier signals and implemented on eleven levels cascaded multilevel inverter under reduced switches topology. The required number of switching pulses generated by considering number of carrier signals is equal to number of switches instead of N-1 carrier signals. This technique allows lower switching transition and it leads to reduced switching losses for topologies utilize minimum number of switches. 1.2 KHz carrier frequency is used to generate switching pulses and verified up to 100 kHz. The Total harmonic distortion is observed for various switching frequencies. The obtained output voltage levels using PD PWM technique proved mathematically. The performance of proposed algorithm is evaluated using Matlab/Simulink.

Keywords– Cascaded Multilevel Inverters, Diagonal dc source, Phase Disposition (PD) PWM Technique.

I. INTRODUCTION

In recent years several topologies are presented for cascaded multilevel inverter under reducing switches concept, some of them are symmetrical and asymmetrical [1]-[10], The advantages of above all structures is the low variety of dc voltage sources, which is the most important feature in determining cost of the inverter [1],Multilevel converters have some particular disadvantages. They need a large number of power semiconductor switches, which increase the cost and control complexity and reduce the overall reliability and efficiency [2].To minimize above mentioned disadvantages number of voltage levels are increased with minimum dc voltage sources and switches. In multilevel inverters the power quality is improved as the number of levels increases at the output voltage and can sustain the operation in case of internal fault [4].Using series and parallel operation of dc voltage sources for eleven levels of output voltage topology presented in [5] utilizes 10switches and 3 dc voltage sources and bus voltage THD is 13.1% but with the topology presented in figure1, 11 voltage levels are obtained using only 9switches and 2 dc voltage sources, therefore the topology presented in Fig1 is smaller because the number of switching devices are reduced .

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PV cells, batteries, capacitors etc. can be used as voltage sources for the presented diagonal dc source cascaded MLI,

The phase disposition technique produces fewer harmonic because it puts harmonic energy directly into a common mode carrier component which cancels across line to line output [6].

In this paper Phase disposition modulation technique is implemented with new algorithm to generate switching pulses to turn on S1, S2, S3, S4, S5 which connects dc voltage sources in series and parallel and the output voltage collected across RL load. In the proposed phase disposition algorithm N-6 carrier signals(equal to switches present in polarity generation circuit) are taken and are compared with sinusoidal reference to achieve gate pulses for generating eleven levels output. It allows lower switching transitions leads to reduced losses in the circuit. The total harmonic distortion observed for varying switching frequencies from1.2kHz to 100 kHz.

II. DIAGONAL DC SOURCE CASCADED MULTI LEVEL INVERTER

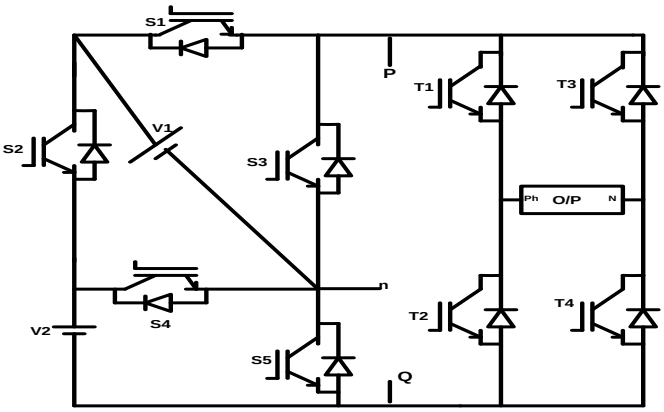

Fig1. Diagonal DC Source Cascaded MLI

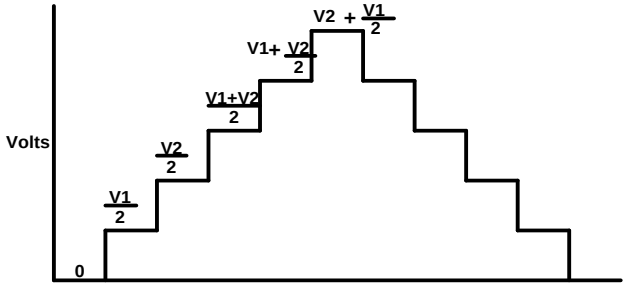

Fig2.Output Voltage across PQ

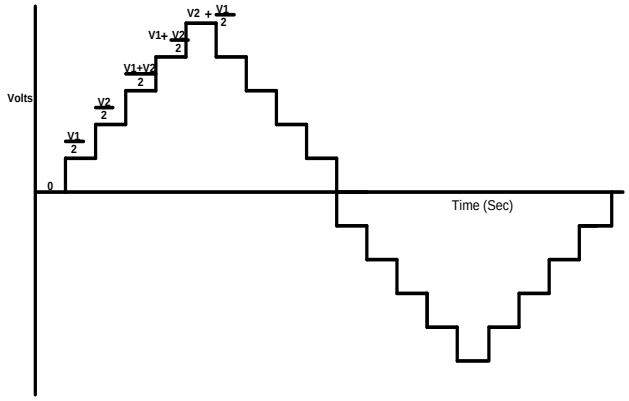

Fig3. Output Voltage across Load

The diagonal dc source cascaded multilevel inverter consist of two circuits (i) Polarity generation is used for generating only positive voltage levels as shown in Fig2. (ii) Polarity conversion circuit is used for converting positive polarity into both positive and negative polarity voltage levels. The output of the polarity conversion circuit is shown in Fig3.
The operation of diagonal dc source cascaded MLI divided into six modes i.e. mode0, mode1, mode2, mode3, mode4, mode5, the switching sequence in every mode and corresponding voltages listed in Table I. The major advantage with the algorithm applied in phase disposition pwm is that the selected switching sequence allows half of the applied voltages across polarity generation circuit, this gives reduced voltage stresses across the switches.

Table 1: Switching Sequence for Eleven Level Diagonal Dc Source Cascaded MLI

Level / Mode	0	1	2	3	4	5
1	**S3, S5**	**S1,S3 ,S5**	**S1,S2, S3 ,S5**	**S1,S2,S5**	**S1,S2,S4 , S5**	**S1,S2,S4**
Output Voltage (Volts)	0	$\frac{V1}{2}$	$\frac{V2}{2}$	$\frac{V1+V2}{2}$	$V1+\frac{V2}{2}$	$\frac{V1}{2}+V2$

III. Mathematical Analysis Of Diagonal DC source Cascaded Mli

During each mode of operation the expected output voltages are calculated by taking each switch resistance 1mΩ using Kirchhoff's laws.

Mode0: When s3 and s5 are switched on the voltage across PQ

$$Vpq = 0 \tag{1}$$

Mode1: When the switches s1, s3, and s5 are turned on the following equations can be written

$$i_1x + i_2x + \ldots..i_nx = V_1 \tag{2}$$

$$i_1x = i_2x = ia \tag{3}$$

$$i_a = \frac{V_1}{2} \tag{4}$$

During this interval the voltage available across Pn is $\frac{V_1}{2}$

Mode2: When s1, s2, s3 and s5are switched on the following ***equation can be written***

$$i_1x + i_2x + ..inx = V_1 \tag{5}$$

$$i_1x = i_2x = i_b \tag{6}$$

$$i_b = \frac{V_1}{2} \tag{7}$$

The voltage present across Pn is $\frac{V_1}{2}$ *and*

$$i_3x + i_4x + \ldots i_nx = V_2 - V_1 \tag{8}$$

$$i_3x = i_4x = ic \tag{9}$$

$$i_c = \frac{V_2 - V_1}{2} \tag{10}$$

From above equation the voltage present across PQ is

$$V_P n + Vn_Q = \frac{V_1}{2} + \frac{V_2 - V_1}{2} = \frac{V_2}{2} \tag{11}$$

Mode4: When switches s1, s2 and s5 are switched on, the following equation can be written

$$i_5x + i_6x + \ldots i_nx = V_2 - V_1 \tag{12}$$

$$i_5x = i_6x = i_d \tag{13}$$

$$i_d = \frac{V_2 - V_1}{2} \tag{14}$$

The voltage present across PQ is

$$V_1 + \frac{V_2 - V_1}{2} = \frac{V_1 + V_2}{2} \tag{15}$$

Mode5: When switches s1, s2, s4, and s5 are switched on

$$2i_7x + i_8x = V_1 \tag{16}$$

$$i_7x + 2i_8x = V_2 \tag{17}$$

Solving above equation we get voltage across PQ is

$$V_{PQ} = V_1 + \frac{V_2}{2} \tag{18}$$

Mode6: when s1,s2 and s4 are turned on the voltage across PQ is

$$V_{PQ} = \frac{V_1}{2} + V_2 \tag{19}$$

where *i1x, i2x, i3x ,…inx* are respective loop currents, *V1,V2, …Vn* voltages applied across respective cell

IV. Proposed Phase Disposition PWM technique Algorithm

In this paper the target is to generate switching pulses for switches S1, S2, S3, and S4and S5 shown in Fig1 at the desired time intervals. First time attempt was made to generate switching pulses using phase disposition pulse width modulation technique, an algorithm is proposed for reducing switches topologies.

In Phase disposition PWM technique N-1 carrier waves are used to generate N level output in conventional cascaded H bridge topologies. But with the proposed algorithm for generation of eleven level cascaded MLI under reduced switches topology the number of triangular carrier signals are equal to number of switches in polarity generation circuit, for generating eleven level only five triangular carrier signals are used.

Five triangular carrier signals are compared with sinusoidal reference signal at their respective time of intervals as shown in Fig4. The selection of triangular carrier frequency plays key role for obtaining required width of pulses. The generated pulses shown in Fig5.This technique greatly reduce the complexity in PWM circuit because of less number of carriers.

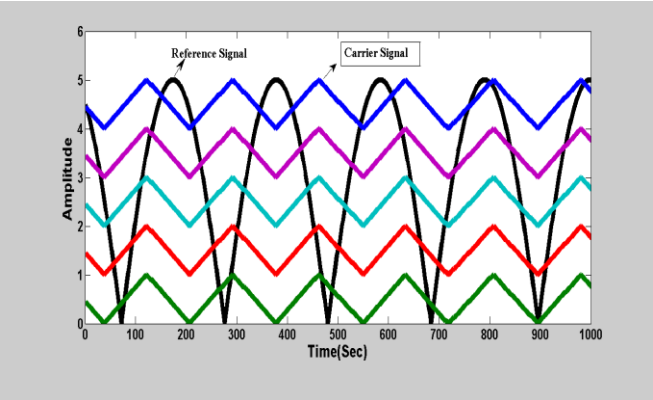

Fig4. Reference and carrier signals in Proposed Phase Disposition PWM Technique for Eleven level Diagonal DC source Cascaded MLI

V. Switching Pulses Generation with The Proposed Phase Disposition PWM Technique Algorithm

The design of the inverter is done using various factors; these factors are obtained from various parameters that contribute the efficiency of inverter

The switching frequency is estimated using frequency modulation index is given by $M_f = \frac{f_c}{f_r}$

where *fc* and *fr* are carrier wave and reference wave frequency.

The amplitude modulation index is defined as

$$M = \frac{V_m}{(n-1)Vc}$$

where the *Vm* peak to peak value of the reference wave and *Vc* are the amplitude of the carrier wave.

The THD is measured as the ratio of all the harmonics in a switching system to the fundamental unit.

$$THD = \frac{\sqrt{\sum_{i=2}^{n} A_i}}{A}$$

where, Ai is the i[th] voltage/current harmonic value. Pulse width modulated systems are usually characterized with power and harmonic losses which result from the switching and conduction losses of the switches/transistors/thyristors that are sed. The losses in the modulation techniques cause the average reduction in phase-phase voltages at each switching frequencies [12].

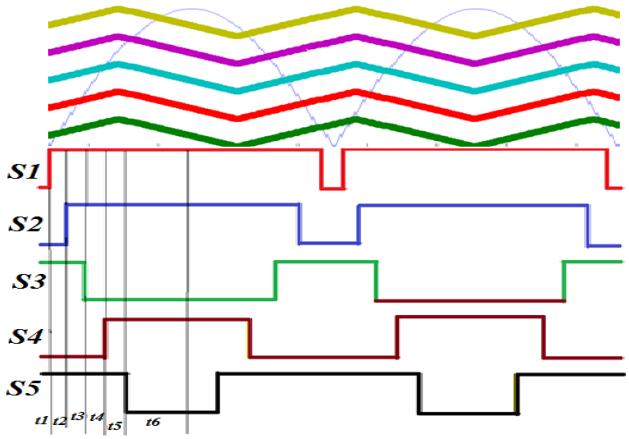

Fig5. Switching Pulses in Proposed Phase Disposition PWM Technique

During each switching interval the magnitude of voltages present across PQ is represented below.

$$0 \le t \le t_1 = 0\ Volts$$

Switches S3, S5 are turned ON

$$t_1 \le t \le t_2 = \frac{V_1}{2}\ Volts$$

Switches S1, S3, S5 are turned ON

$$t_2 \le t \le t_3 = \frac{V_2}{2}\ Volts$$

Switches S1, S2, S3, and S5 are turned ON

$$t_3 \le t \le t_4 = \frac{V_1 + V_2}{2}\ Volts$$

Switches S1, S2, S5 are turned ON

$$t_4 \le t \le t_5 = V_1 + \frac{V_2}{2}\ Volts$$

Switches S1, S2, S4, and S5 are switched ON

$$t_5 \le t \le t_6 = \frac{V_1}{2} + V_2\ Volts$$

Switches S1, S2, S4 are switched ON

The above obtained voltage magnitudes during each interval are verified mathematically in section III and obtained voltage magnitudes matching with the simulated results.

VI. Simulation Circuit

The diagonal dc source cascaded multilevel inverter circuit shown in Fig1. To generate switching pulses Phase disposition PWM technique is employed. For generating required number of switching pulses under proposed algorithm the below Matlab/Simulink circuit is designed. To

generate five switching pulses, five carrier signals compared with the positive peak of the sinusoidal signal. All carrier signals switching frequency is selected as 1.2 kHz and 50 Hz reference signal is compared with the carrier signals as shown in Fig6. The wave forms observed for a modulation index unity.

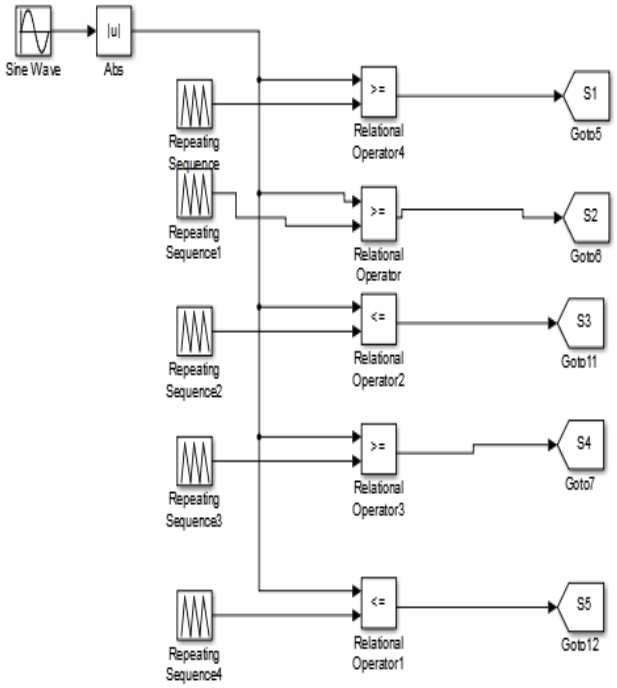

Fig6. Phase Disposition PWM Circuit for generating switching pulses with the proposed algorithm

VII. Simulation Results

The proposed algorithm for Phase Disposition PWM technique simulated using Matlab /Simulink R2013 version. For observing proposed algorithm to generate required switching pulses eleven level diagonal dc source cascaded multilevel inverter is considered with RL load as R=45Ω and L=55mH. It was observed that with the proposed algorithm the THD is reduced. For the voltage wave the THD is 14,21% and the current THD is 9.66%. It is observed that the voltage THD is slightly increasing with the switching frequency at 100 kHz and the current THD is reducing with the switching frequency at 100 kHz switching frequency its value is only 0.73%. Results obtained with proposed algorithm are shown with their THD in Fig7, Fig8, Fig9 and Fig10.

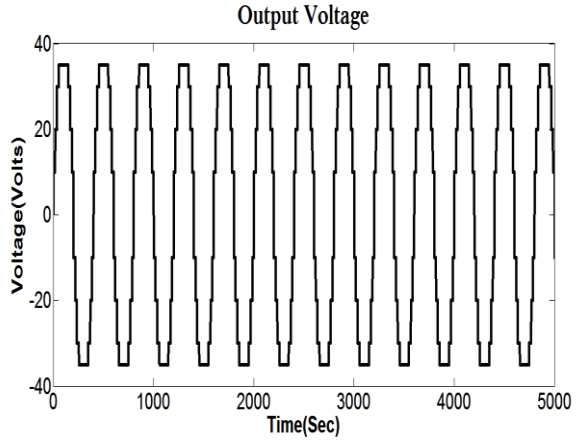

Fig7. 11 level Output voltage with proposed Phase Disposition (PD) algorithm

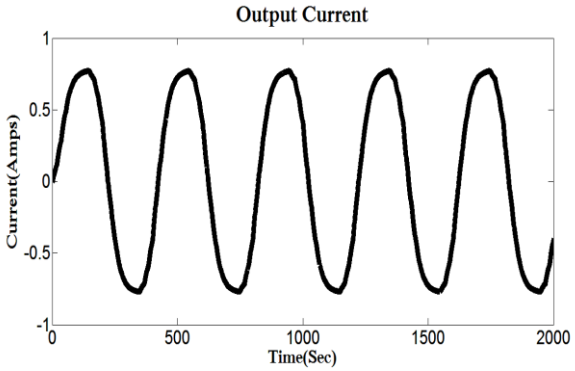

Fig8. Output Current with proposed Phase Disposition (PD) algorithm

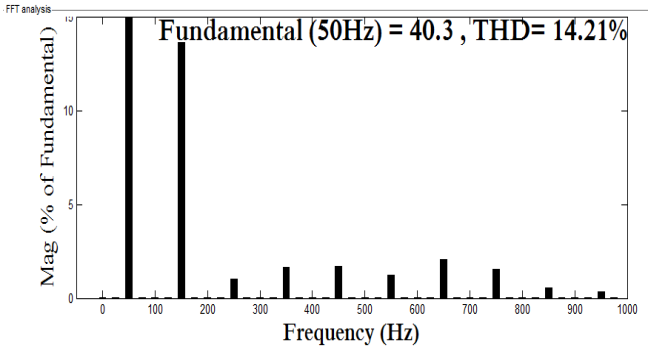

Fig9. 11 level Output voltage THD with proposed Phase Disposition (PD) algorithm

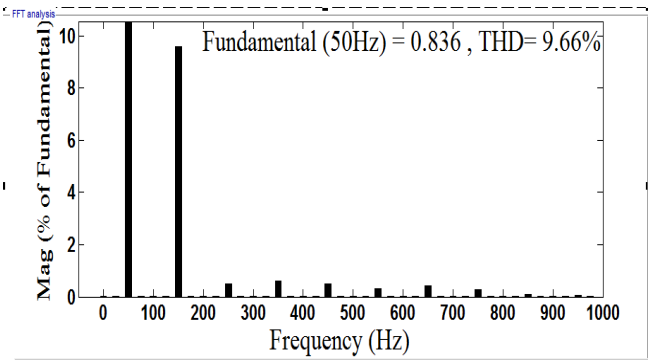

Fig8. Output Current THD with proposed Phase Disposition (PD) algorithm

VIII. Conclusion

In this paper new algorithm was proposed to Phase Disposition PWM technique and implemented on diagonal dc source cascaded multilevel inverter under reduced switches topology and it was verified for switching frequencies of 1.2kHz, 5kHz, 10kHz and 100kHz at unity modulation index using Matlab/Simulink. The proposed modulation technique increase the number of levels with reduction of carrier signals. In the future the Simulink results are verified with hardware prototype.

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BIOGRAPHIES

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M.Sushama was born in 1973, in Nalgonda district, Telangana state. India. Obtained B.Tech degree in 1993 and M.Tech degree in 2003, specialization in Electrical Power Systems from JNTU, INDIA. She obtained her Ph.D. from JNTU Hyderabad, in 2009 in the area of "Power Quality" using Wavelet Transforms. She has more than 22 years of teaching experience and at present she is working as head and professor in the department of electrical and electronics engineering, JNTUH, Hyderabad, India. Her research interests includes green energy, power systems, power electronics, facts controllers and power quality and harmonics.

Mitigation of PQ Disturbances using Unit-Template Control Algorithm based DSTATCOM

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Abstract–This paper presents unit-template based control algorithm for Distributed Static Compensator (DSTATCOM) to mitigate Power Quality (PQ) disturbances in the three phase distribution system. The proposed DSTATCOM can be operated in Power Factor Correction (PFC) and Zero Voltage Regulation (ZVR) modes to mitigate PQ disturbances such as elimination harmonics, load balancing, unity power factor at the source and terminal voltage regulation. The main feature of this unit template control Algorithm is it requires only five sensors whereas conventional control algorithm requires ten sensors which reduces the cost of DSTATCOM. In this paper, four-leg VSC based DSTATCOM is used for neutral current compensation. The main advantage of four-leg VSC is eliminating transformer at Point of Common Coupling (PCC) which also reduces cost of DSTATCOM. The unit template based control algorithm for DSTATCOM is modeled in MATLAB environment using Simulink and Sim Power System (SPS) toolboxes and results are validated.

Keywords–DSTATCOM, Unit Template Control Algorithm, Power Quality, neutral current compensation.

I. INTRODUCTION

The use of power electronic converters is increasing in day to day life because they are energy efficient, compact and reliability compared to other systems [1]-[2].But main disadvantage of these power electronic converter are generates harmonic currents at source as well as load which effects performance of distribution system. These harmonic currents are responsible for drawing more reactive power from AC source and which causes voltage distortion and loss in the three-phase distribution system [3]. Power Quality (PQ) problems are defined in terms of deviation in voltage/current waveforms, unbalance, distortion, reactive power drawn [4].Many standards and guidelines are used in the design of power systems with nonlinear loads [5]-[6].

The performance of shunt connected device namely DSTATCOM depends upon control algorithm and design of its power circuit [7]-[9]. The performance of DSTATCOM depends on the selection of interfacing of ac inductor, DC bus capacitor and IGBTs [10].The various control algorithms reported in the literature are sinusoid-tracking algorithm [11], parallel neural network based algorithm [12],ABC theory based control algorithm [13],repetitive control algorithm [14],delta modulation based control [15], Icosφ control algorithm[16] and simulation study of EPLL-based control has been reported for power factor correction in single phase ac system[17].These control algorithms require ten feedback sensors whereas proposed unit-template control algorithm requires five feedback sensors. Kasal et al [18] proposed voltage and frequency controller for isolated asynchronous generators feeding three-phase four-wire loads using reduced feedback sensors.

In this paper, a unit-template control algorithm is proposed for the control of a four-leg VSC based DSTATCOM for Power Factor Correction (PFC) and Zero Voltage Regulation (ZVR) modes of operation. During PFC and ZVR modes of proposed algorithm PQ problems such as elimination of harmonics, load balancing, and unity power factor at source, reactive power control and neutral current compensation are mitigated [19]. The proposed algorithm reduces the number of feedback sensors which reduces cost of DSTATCOM. The four-leg VSC based DSTATCOM is used for neutral current compensation which eliminates transformer connection at PCC. The computer simulation results of unit-template control algorithm for four-leg VSC based DSTATCOM are validated under MATLAB environment using Simulink and Simpower System (SPS) toolboxes.

II. SYSTEM CONFIGURATION AND PRINCIPLE OF OPERATION

The schematic diagram of four-leg VSC based DSTATCOM feeding three-phase four-wire linear/non-linear load along with unit-template control algorithm is shown in Fig.1.The distribution system linear loads consist of three- phase star-connected resistive load and non-linear loads consist of three single-phase diode bridge rectifiers with R-C load. These non-linear loads in the distribution system will create PQ problems at the source without DSTATCOM. To mitigate PQ problems a DSTATCOM is connected at Point of Common Coupling (PCC). The proposed DSTATCOM consists of four-leg IGBT based voltage source converter (VSC), four interface inductors and a dc bus capacitor. The four-leg VSC based DSTATCOM will inject compensating currents (i_{ca}, i_{cb}, i_{cc}) in such a way that source current (i_{sa}, i_{sb}, i_{sc}) is pure sinusoidal and maintains unity power factor at source. A ripple of Resistance (R_f) and Capacitor (C_f) is connected at PCC to filter voltage harmonics at three phase source voltages (v_{sa}, v_{sb}, v_{sc}).

III. PROPOSED UNIT-TEMPLATE CONTROL ALGORITHM

The performance of DSTATCOM depends upon quick and accurate extraction of fundamental of source current harmonic components. All basic control algorithms of custom power devices require ten feedback sensors whereas proposed control algorithm requires only five feedback sensors. The basic control algorithms require three feedback

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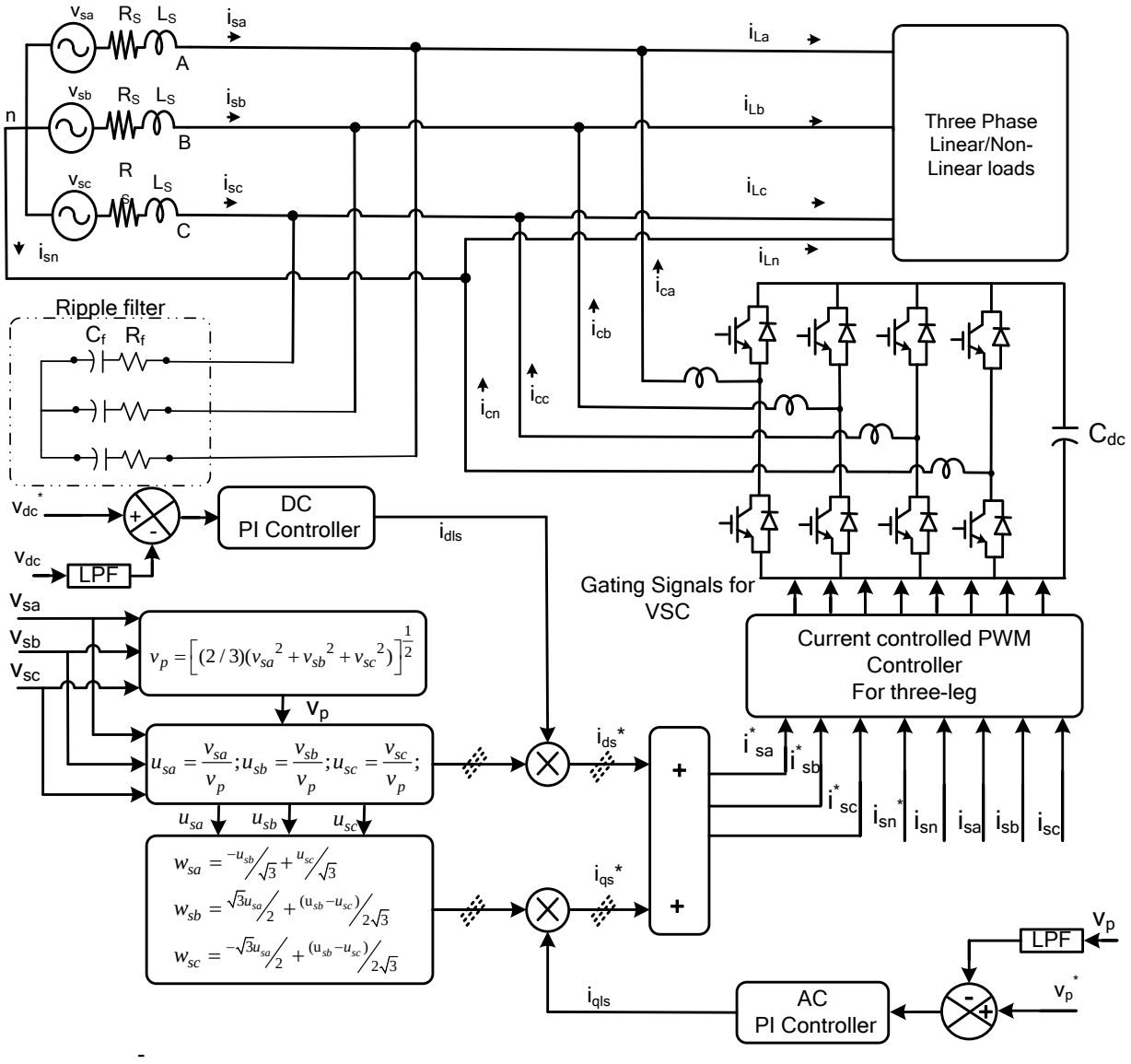

Fig.1Unit-template control algorithm of four-leg VSC based DSTATCOM

sensors for load currents, three feedback sensors for source voltages, one feedback sensor for dc bus voltage and three feedback sensors for source currents. The unit-template control algorithm requires two feedback sensors for source voltages (v_{sa}, v_{sb}), one feedback sensor for dc bus voltage (v_{dc}) , two feedback sensors for source currents(i_{sa},i_{sb}) and the third phase voltage v_{sc}(-(v_{sa}+v_{sb})) & current i_{sc}(-(i_{sa}+i_{sb})).The main feature of unit template control algorithm is to reduce number of feedback sensors which will improve performance of DSTATCOM. The proposed unit-template control algorithm based DSTATCOM is the effective solution to mitigate harmonics, power factor correction, load unbalancing, reactive power control and neutral current compensation.

The supply voltages (v_{sa}, v_{sb}, v_{sc}) of three-phase system can be represented as

$$v_{sa} = v_{mp}\sin(wt) \tag{1}$$

$$v_{sb} = v_{mp}\sin(wt - 120^o) \tag{2}$$

$$v_{sc} = v_{mp}\sin(wt - 240^o) \tag{3}$$

The magnitude of three phase voltages (v_{sa}, v_{sb}, v_{sc}) at PCC is given by

$$v_p = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \tag{4}$$

A. Power Factor Correction operation of Unit Template based DSTATCOM

The in-phase component of unit templates (u_{sa},u_{sb},u_{sc}) are calculated from (v_{sa},v_{sb},v_{sc}) which are given by

$$u_{sa} = \frac{v_{sa}}{v_p}; u_{sb} = \frac{v_{sb}}{v_p}; u_{sc} = \frac{v_{sc}}{v_p}; \quad (5)$$

The dc bus voltage error (v_{edc}) is the difference between reference dc bus voltage (v_{dc}^*) and sensed dc bus voltage (v_{dc}) under PFC mode. This dc voltage error is given to dc bus Proportional Integral (PI) controller and its output of PI is considered as active component of current loss (i_{dls}).

$$i_{dls(k)} = i_{dls(k-1)} + K_{dp}(v_{edc(k)} - v_{edc(k-1)}) + K_{di}v_{edc(k)} \quad (6)$$

where K_{dp} and K_{di} are proportional and integral gain constants of DC bus PI controller.

The reference active component source currents (i_{dsa}^*,i_{dsb}^*,i_{dsc}^*) are determined as

$$i_{dsa}^* = u_{sa}i_{dls}; i_{dsb}^* = u_{sb}i_{dls}; i_{dsc}^* = u_{sc}i_{dls}; \quad (7)$$

B. Zero Voltage Regulation operation of Unit Template based DSTATCOM

The quadrature phase component of unit templates (w_{sa},w_{sb},w_{sc}) are calculated from (u_{sa}, u_{sb}, u_{sc}) which are given by

$$w_{sa} = \frac{(-u_{sb} + u_{sc})}{\sqrt{3}}; \quad (8)$$

$$w_{sb} = \frac{(\sqrt{3}u_{sb} + u_{sb} - u_{sc})}{2\sqrt{3}}; \quad (9)$$

$$w_{sc} = \frac{(-3u_{sa} + u_{sb} - u_{sc})}{2\sqrt{3}}; \quad (10)$$

The ac bus voltage error (v_{ep}) is the difference between reference ac bus voltage (v_p^*) and sensed ac bus voltage at PCC (v_p) under ZVR mode. This ac voltage error is given to ac bus Proportional Integral (PI) controller and its output of PI is considered as reactive component of current loss (i_{qls}).

$$i_{qls(k)} = i_{qls(k-1)} + K_{qp}(v_{ep(k)} - v_{ep(k-1)}) + K_{qi}v_{ep(k)} \quad (11)$$

where K_{qp} and K_{qi} are proportional and integral gain constants of AC bus PI controller.

The reference reactive component source currents (i_{qsa}^*,i_{qsb}^*,i_{qsc}^*) are determined as

$$i_{qsa}^* = w_{sa}i_{qls}; i_{qsb}^* = w_{sb}i_{dls}; i_{qsc}^* = w_{sc}i_{qls}; \quad (12)$$

C. *Generation of Reference source currents*

The total reference source currents (i_{sa}^*,i_{sb}^*,i_{sc}^*) are the sum of the reference in-phase source current (i_{dsa}^*,i_{dsb}^*,i_{dsc}^*) and reference quadrature source currents(i_{qsa}^*,i_{qsb}^*,i_{qsc}^*)are

$$i_{sa}^* = i_{dsa}^* + i_{qsa}^* \quad (13)$$

$$i_{sb}^* = i_{dsb}^* + i_{qsb}^* \quad (14)$$

$$i_{sc}^* = i_{dsc}^* + i_{qsc}^* \quad (15)$$

D. Current Controlled PWM Generator

In a current controlled PWM Generator, the difference between reference source currents (i_{sa}^*, i_{sb}^*, i_{sc}^*) and sensed source currents (i_{sa}, i_{sb}, i_{sc}) are taken as error source currents in each of the three phases. In addition to error source currents in three phases, the source neutral currents(i_{sn}) are compared with triangular waveform to generate switching pulses for four-leg VSC based DSTATCOM.

IV. Results and Discussion

MATLAB/SIMULINK is used for development of proposed DSTATCOM and results are carried out with ode23tb solver (stiff/TR-BDF-2) in discrete mode at fixed step size of 4 × 10−6.The performance of unit-template control algorithm based DSTATCOM is simulated in PFC and ZVR modes of operation at three phase time-varying linear/nonlinear loads.

A. Performance of unit template control algorithm

Fig.2shows the various intermediate signals of unit template control algorithm which include three phase source voltage (v_s), three phase load current (i_L), three phase reference source current (i_s^*), reference active component source currents (i_{dsa}), reference reactive component source currents (i_{qsa}), active component of current loss (i_{dls}), reactive component of current loss (i_{qls}), DC bus voltage error (v_{edc}), AC bus voltage error (v_{ep}) and three phase sensed source (i_s) respectively. The waveforms of unit template control algorithm shows that fast and accurate extraction of control signals occurs at three phase non-linear loads in ZVR mode.

B. Performance of DSTATCOM in PFC Mode

The performance of four-leg VSC based DSTATCOM for PFC mode with three phase linear load is shown in Fig.3.The dynamic performance of DSTATCOM is analyzed on the basis of three phase source voltages (v_s), three phase source currents (i_s), three phase load currents (i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents (i_c), load neutral current (i_{Ln}), source neutral current (i_{sn}), sensed dc link voltage (v_{dc}) & reference dc link voltage (v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC (v_p*) are shown in Fig.3 under a time varying load at t=0.62sec to 0.78 sec condition. The waveforms show that satisfactory operation of DSTATCOM in PFC mode operation under linear loads.

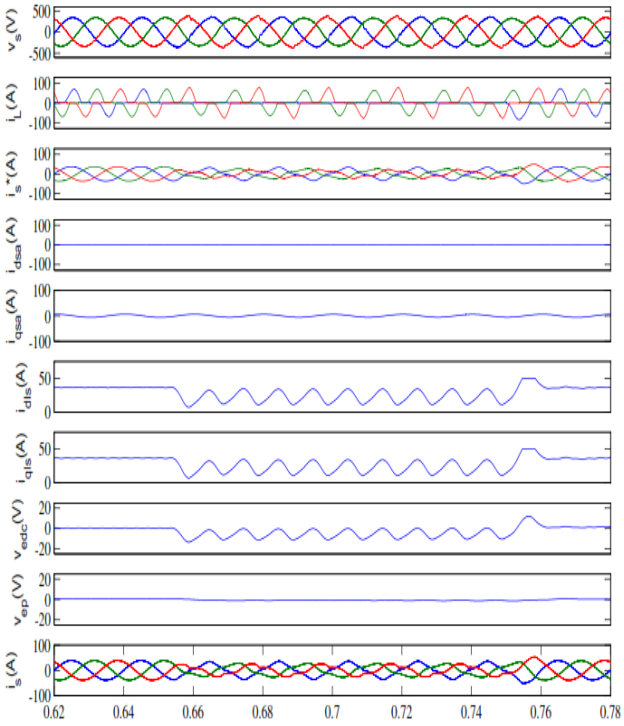

Fig. 2.Various intermediate signals of unit template control algorithm

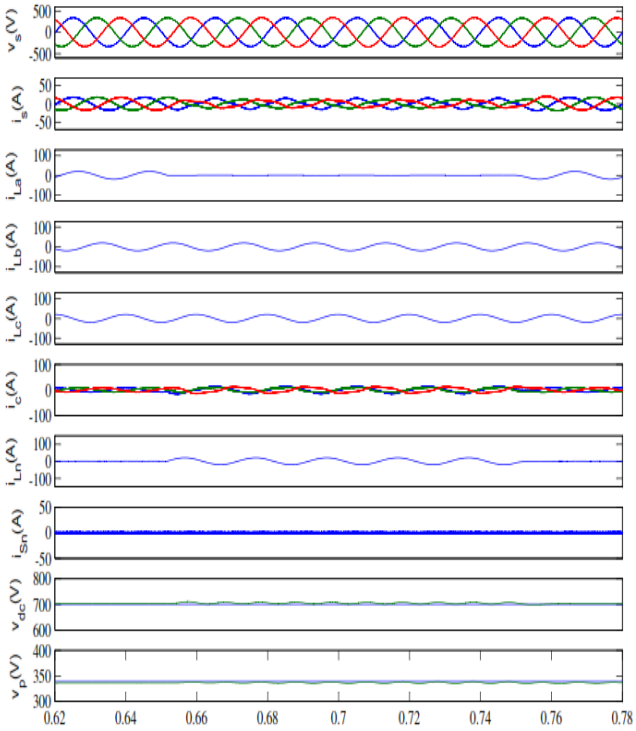

Fig. 3.Dynamic performance of DSTATCOM under linear loads in PFC mode

Similarly the performance of four-leg VSC based DSTATCOM for PFC mode with three phase non-linear loads/(diode bridge rectifier with parallel connected resistive and capacitive load) considered in the distribution system is shown in Fig.4. The waveforms of three phase source voltages (v_s), three phase source current (i_s), three phase load currents(i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents (i_c), load neutral current (i_{Ln}), source neutral current (i_{sn}), sensed dc link voltage(v_{dc}) & reference dc link voltage(v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC(v_p*) are shown in Fig.4. The harmonic spectra waveforms of phase 'a' source voltage(v_{sa}), source current (i_{sa}) and load current harmonic(i_{La}) with three phase non-linear R-C loads are shown in Fig.5(a)-5(c).The waveforms shows that the %THD of phase 'a' load current (i_{La}) is 70.74% whereas %THD of source voltage(v_{sa}) and source current(i_{sa}) are 2.23%,4.96% respectively. The performance results of DSTATCOM in PFC modes operation are shown in Table.1. It is observed that the proposed DSTATCOM shows give satisfactory results in PFC mode operations under non-linear loads.

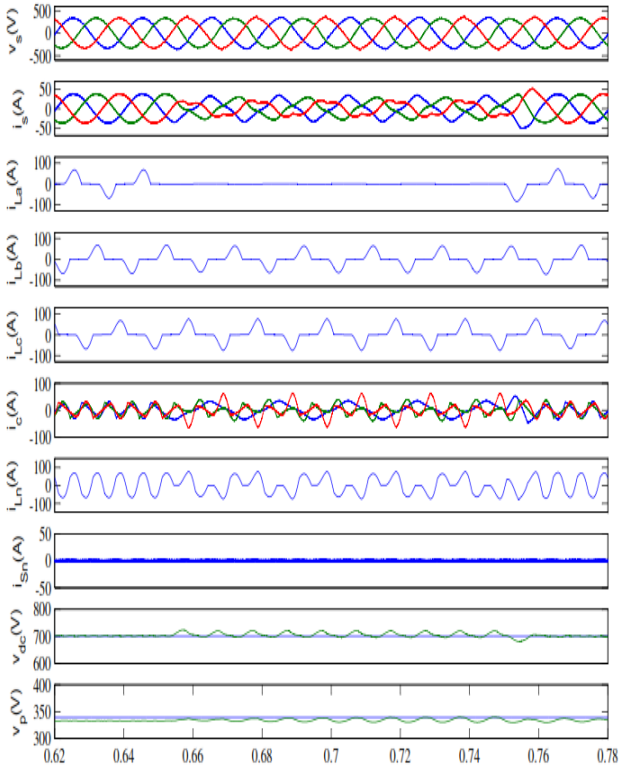

Fig.4 Dynamic performance of DSTATCOM under non-linear loads in PFC mode

C. Performance of DSTATCOM in ZVR Mode

In ZVR modes operation, the amplitude of reference terminal voltage at PCC is regulated to the reference terminal voltage by injecting extra reactive power. The dynamic performance of DSTATCOM is analyzed on the basis of three phase source voltages(v_s), three phase source current (i_s),three phase load currents(i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents(i_c), load neutral current (i_{Ln}), source

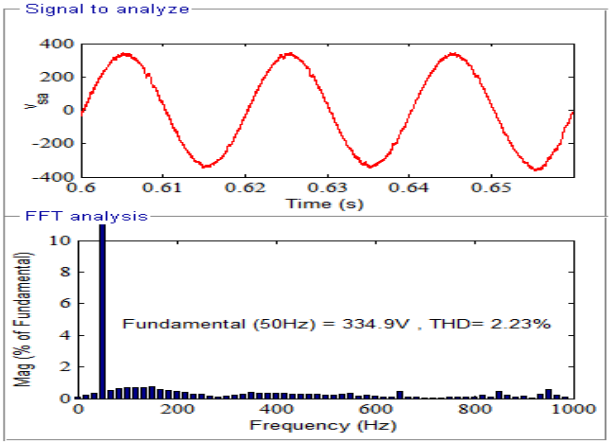

Fig. 5(a) Harmonic Spectrum of phase 'a' source voltage in PFC mode

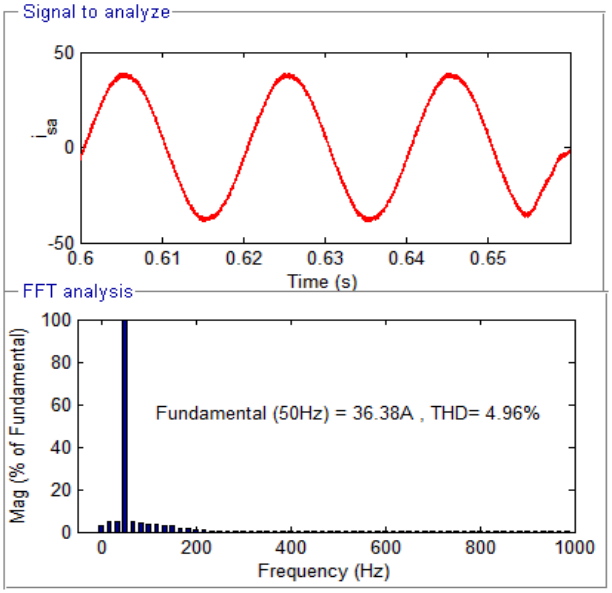

Fig. 5(b) Harmonic Spectrum of phase 'a' source current in PFC mode

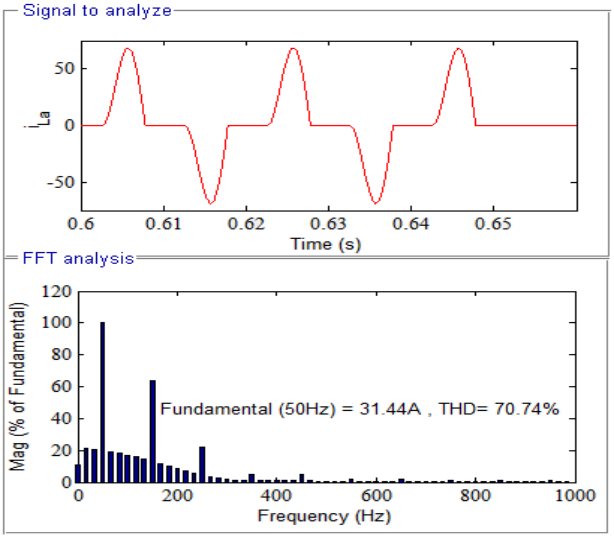

Fig. 5(c) Harmonic Spectrum of phase 'a' load current in PFC mode

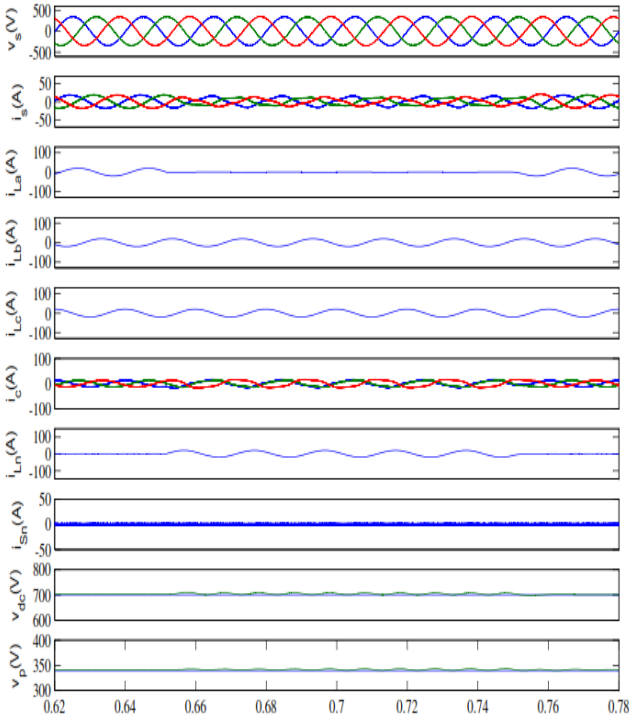

Fig.6.Dynamic performance of DSTATCOM under linear loads in ZVR mode

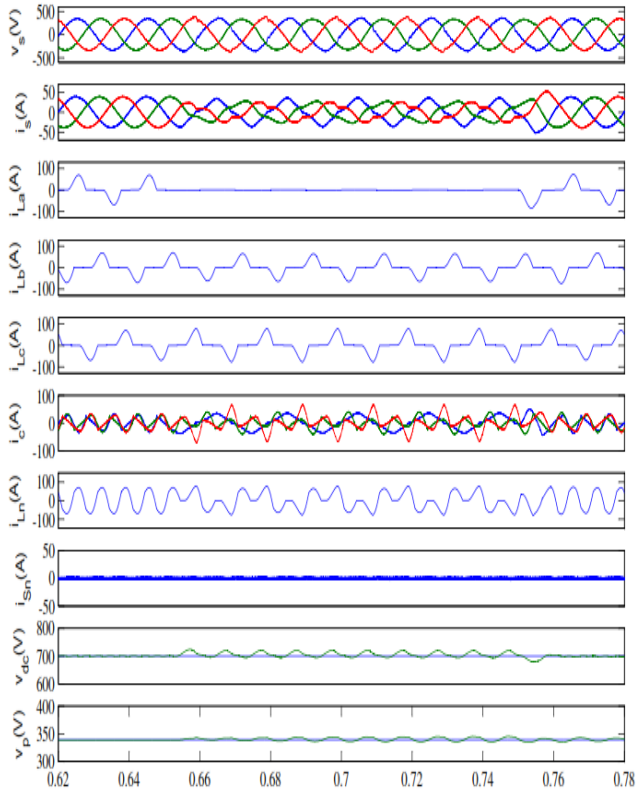

Fig.7.Dynamic performance of DSTATCOM under non-linear loads in ZVR mode

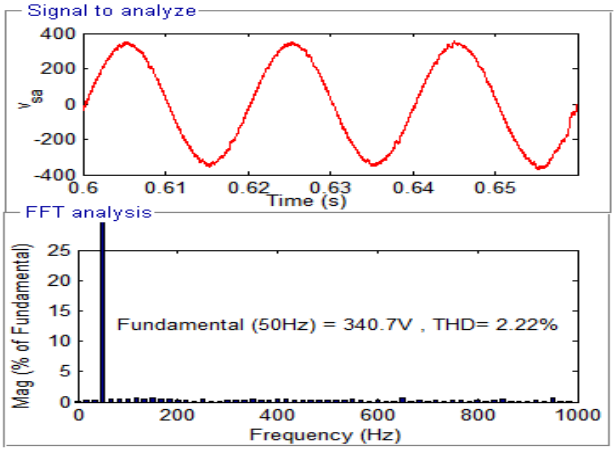

Fig.8(a) Harmonic Spectrum of phase 'a' source voltage in ZVR mode

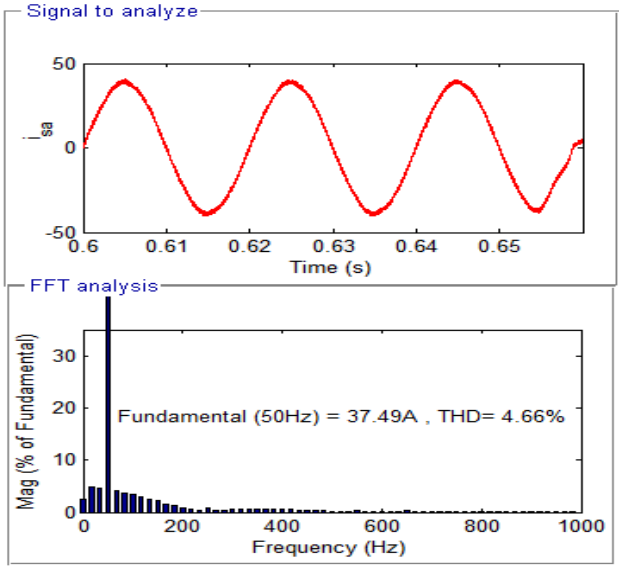

Fig. 8(b) Harmonic Spectrum of phase 'a' source current in ZVR mode

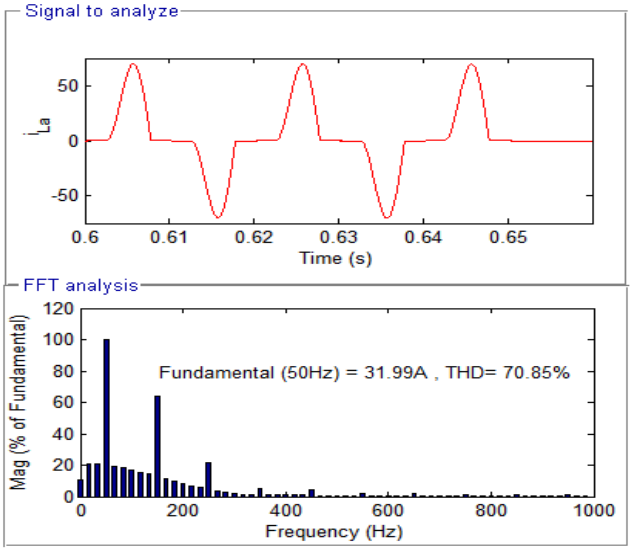

Fig. 8(c) Harmonic Spectrum of phase 'a' load current in ZVR mode

neutral current (i_{sn}), sensed dc link voltage (v_{dc}) & reference dc link voltage (v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC(v_p*) are shown in Fig.6 under a time varying load at t=0.62sec to 0.78 sec conditions. The waveforms show that satisfactory operation of DSTATCOM in ZVR mode operation under three phase linear loads.

The performance of four-leg VSC based DSTATCOM for PFC mode with three phase non-linear load is shown in Fig.7. The waveforms of three phase source voltages (v_s), three phase source current (i_s), three phase load currents (i_{La}, i_{Lb}, i_{Lc}), three phase compensating currents(i_c), load neutral current (i_{Ln}), source neutral current(i_{sn}), sensed dc link voltage(v_{dc}) &reference dc link voltage(v_{dc}*) and sensed terminal voltage at PCC(v_p) and reference terminal voltage at PCC(v_p*) are shown in Fig.7.The harmonic spectra waveforms of phase 'a' source voltage (v_{sa}) ,source current(i_{sa}) and load current harmonic(i_{La}) are shown in Fig.8(a)-8(c).The waveforms shows that the %THD of phase 'a' load current (i_{La}) is 70.85% whereas %THD ofsource voltage (v_{sa}) and source current (i_{sa}) are 2.22%, 4.66% respectively. The performance results of DSTATCOM in ZVR modes operation are shown in Table.1. It is observed that the proposed DSTATCOM shows give satisfactory results in ZVR mode operations under three phase non-linear loads. The DSTATCOM is able to regulate reference terminal voltage at PCC of 339V.

Table.1.Performance of DSTATCOM at PFC and ZVR modes of operations

Operating Mode	Performance Parameters	Non-Linear R-C Load
PFC Mode	Source voltage(v_{sa}), %THD	334.9V, 2.23%
	Source current (i_{sa}), %THD	36.38A, 4.96%
	Load current (i_{La}), %THD	31.44A, 70.74%
ZVR Mode	Source voltage(v_{sa}), %THD	340.7V, 2.22%
	Source current (i_{sa}), %THD	37.49A, 4.66%
	Load current (i_{La}), %THD	31.99A, 70.85%

V. CONCLUSION

The proposed unit template control algorithm for four-leg VSC based DSTATCOM has been found to provide acceptable characteristics in PFC and ZVR modes of operation. During the PFC and ZVR modes of operations, the dynamic performance of DSTATCOM shows satisfactory results for harmonic elimination, reactive power control, load balancing, and neutral current compensation

under linear and non-linear loads. The DC link voltage and terminal voltage at PCC of proposed DSTATCOM has been also regulated without overshoot to reference value under various load conditions. It is observed that the %THD of source current and source voltage is within IEEE519 standard.

APPENDIX

Three phase supply voltage=415V, 50Hz.
Supply Impedance: R_s=0.05Ω, L_s=5mH
Loads: Linear Loads R=15Ω and L=25mH
Non-Linear R-C Loads: three single phase diode bridge rectifier with R=15Ω and C=500µF
DC bus Capacitor C_{dc}=3000 µF
PWM switching frequency f_s=10 KHz
DC bus PI Controller: K_{dp}=2.36 K_{di}=4.1
AC bus PI Controller: K_{qp}=1.02 K_{qi}=2.41

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BIOGRAPHIES

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Load Conductance Estimation Based Control Algorithm for Shunt Connected Custom Power Devices

Vishal E. Puranik[1] Sabha Raj Arya[1]

Abstract-In this paper, a control algorithm is developed for three phase DSTATCOM (Distribution Static Compensator). It is based on load conductance estimation through the fundamental load power calculation using second order generalized integrator (SOGI). Developed three phase system is simulated in power factor correction (PFC) and zero voltage regulation (ZVR) modes. In PFC mode, it provides compensation for reactive power, harmonics and load balancing whereas in ZVR mode it regulates the PCC voltage along with the harmonics elimination and load balancing. The simulation results are found satisfactory with the proposed control algorithm under dynamic loading conditions.

Keywords-Conductance, Susceptance, SOGI, Unit templates, ZVR.

I. INTRODUCTION

Power quality disturbances like harmonics, unbalanced load, voltage dips, flicker, etc are increasing every year [1]. It affects not only the performance of various power system components but also economy of electricity market [2]. Improved power quality is an important demand of distribution system [3-5]. Power quality issues are generated in distribution side by consumers, so it is desired to attenuate them at distribution side and this is achieved by custom power devices [6,7]. DSTATCOM is a shunt connected device which can be operated in PFC as well as ZVR mode [8]. It provides compensation for reactive power, harmonics as well as balances load and regulates voltage. Various topologies of DSTATCOM has been proposed in literature for three phase three wire and three phase four wire distribution system[9]. Effective use of DSTATCOM depends on its parameter design as per system requirement [10]. The dynamic and steady performance of DSTATCOM is decided by control algorithm used for generation of compensation currents.

Mindykowski *et al.* [11] have reported new concept based on instantaneous reactive power theory in ship electrical power system. It is based on mean value instead of traditional low pass filter under non-ideal ac mains. Singh *et al.* [12] have discussed basic control algorithm based on peak detection in four wire system. The implementation of SRF theory based in hybrid active filter is reported in the literature [13,14]. Massoud *et al.* [15] have reported a review on control algorithm used for shunt active compensation. In this paper control algorithms are divided in time domain and frequency domain. Again, in time domain control algorithm, various control algorithms are reported using different classical approaches. Detailed configuration, control and various topologies are reported in the literature [16, 19]. Kunjumuhammed and Mishra [20] have reported a new control algorithm in non stiff supply source with detailed synchronizing circuit of active filter during operation. It is based on power calculations in signal phase circuit. Shu *et al.* [21] have reported field-programmable gate array (FPGA) plated form for implementation of active filter. This platform has integrated whole procedure related to signal processing. Second order generalized integrator based extraction of fundamental line voltage under distorted condition algorithm for a single phase shunt active power filter has been proposed. Ciobotaru *et al.* [22] have proposed single phase SOGI-PLL with simple structure. It is able to provide information related to phase, amplitude and frequency of supply source for converter application. It can generate orthogonal system voltage without any delay. It is also adaptive with respect to frequency variations. Golestan *et al.* [23] have discussed structure, analysis and application of SOGI PLL in single phase active filter. Another application of SOGI [24] is reported in grid synchronization system where it is cable of providing desire response for the estimation of symmetrical components of PCC voltage under non ideal condition.

In this paper, Second order generalized integrator (SOGI) [22-24] is used in three phase three wire system for extraction of active and reactive component of load currents. Further, load physical parameters (conductance and susceptance) are estimated by calculating the fundamental power flowing from PCC to load. This algorithm presents a simpler way of calculating the load conductance and the generation of supply reference current. All parameters of control algorithm has physical meaning, it does not involve any assumption of parameters. Good detection accuracy, fast dynamic performance, simpler calculations are features of this control algorithm.

II. SYSTEM CONFIGURATION

Fig.1 shows schematic of 3 leg VSC-based DSTATCOM connected to a three phase three wire distribution system, where an ac source with impedance (Zs) is feeding a non linear load. The L_f are an interfacing inductors connected on ac side of VSC, used for reducing the ripples in the current. A series combination of R_f-C_f are connected at point of common coupling (PCC) in parallel with the load circuit. It is a first order high pass passive filter used for filtering higher order switching harmonics produced by VSC. The C_{dc} is a DC link capacitor with voltage V_{dc} , which is regulated by PI regulator in DC link. The phase PCC voltages (v_{sa},v_{sb},v_{sc}), load currents (i_{La}.i_{Lb},i_{Lc}) and supply currents (i_{sa},i_{sb},i_{sc}) are sensed and fed to control algorithm.

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The DSTATCOM currents (i_{fa},i_{fb},i_{fc}) are injected to compensate the reactive and harmonic components present in the load current.

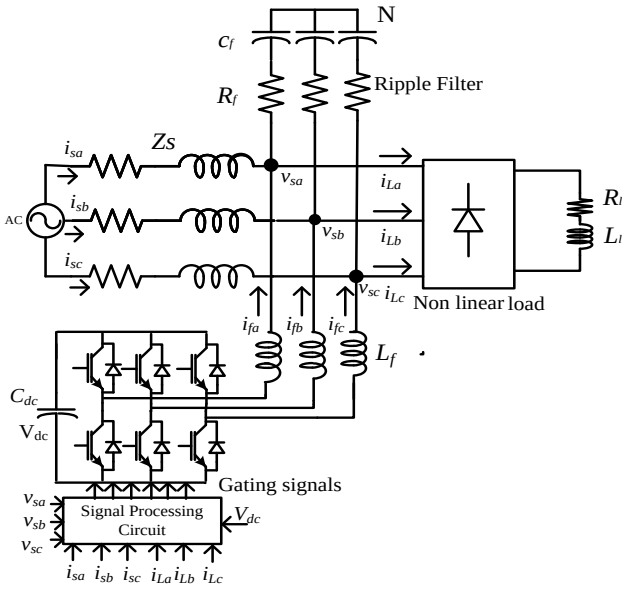


Fig.1. Schematic diagram of 3 Leg VSC-based DSTATCOM

III. Control Algorithm

Fig. 2 shows the block diagram of estimation of reference supply currents based on conductance factor. In this algorithm PCC voltages (v_{sa},v_{sb},v_{sc}), load currents (i_{La}.i_{Lb},i_{Lc}) and supply currents (i_{sa},i_{sb},i_{sc}) are required for the extraction of reference supply currents (i_{sa}^*,i_{sb}^*,i_{sc}^*).Mathematical expressions used in control algorithm for the extraction of various control parameters are discussed as follows.

A. Extraction of Fundamental Active and Reactive Component from Distorted Load Current Using SOGI

Fig. 3 indicates block diagram of SOGI where load current is given as an input to SOGI. I_r and I_q are the fundamental in phase and quadrature components of currents. Transfer function of SOGI block is written as [22-24],

$$T.F. = \frac{i_1(s)}{i_L(s)} = \frac{k\omega s}{s^2 + \omega^2 + k\omega s} \qquad (1)$$

where k is gain parameter, ω is the frequency of the desired frequency component to be extracted, in this case it is 314 rad/sec.

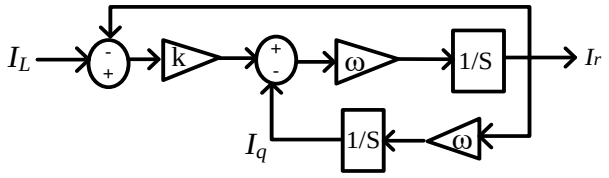


Fig.3 Second Order Generalized Integrator

Performance of SOGI totally depends on value of k. Changing load condition like increase or decrease in load current or harmonic contents causes some delay to stabilize output of SOGI. Dynamic response of SOGI is observed with a step input by putting various values of gain (k) in time domain.

Fig.4 shows the response of SOGI to unit step input. It is found that for higher values of 'k' dynamics of SOGI is faster. Similarly filtering performance of SOGI also depends on value of 'k'. It is found that more the lower values of 'k', bandwidth hence better filtering performance. Another side larger value of k is not able to give require bandwidth and the quality of extracted frequency component gets deteriorated. From the above analysis, it is found that there is a tradeoff between dynamic performance and filtering performance. Here the value of k is selected as 1, so that dynamic is quite fast and filtering performance is also satisfactory.

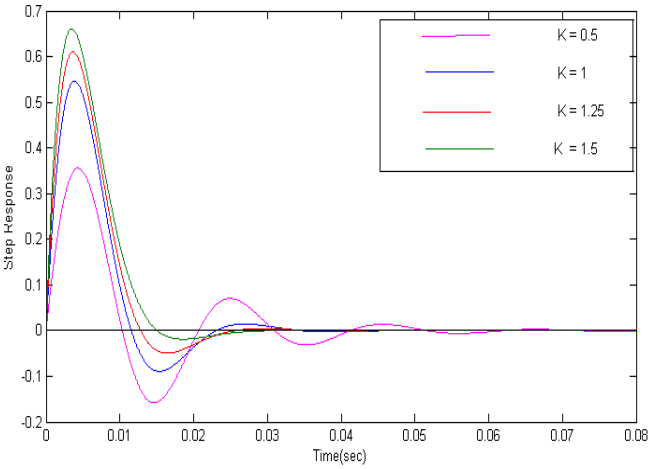


Fig.4 Step response of second order generalized integrator (SOGI)

After putting value of 'k' and w transfer function of SOGI becomes

$$T.F. = \frac{i_1(s)}{i_L(s)} = \frac{k\omega s}{s^2 + \omega^2 + k\omega s} \qquad (2)$$

It is second order system, its characteristic equation can be written as,

$$s^2 + 314s + 314^2 = 0 \qquad (3)$$

Poles of transfer function come out to be (-157+j271.93) and (-157-j271.93), which are located on left half of 's' plane hence for the selected value of k and w response of SOGI is stable.

The various calculations of SOGI based control algorithm is given below.

The PCC voltages (v_{sa},v_{sb},v_{sc}) are sensed to calculate in phase and quadrature unit templates as follows [12].

$$v_t = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \qquad (4)$$

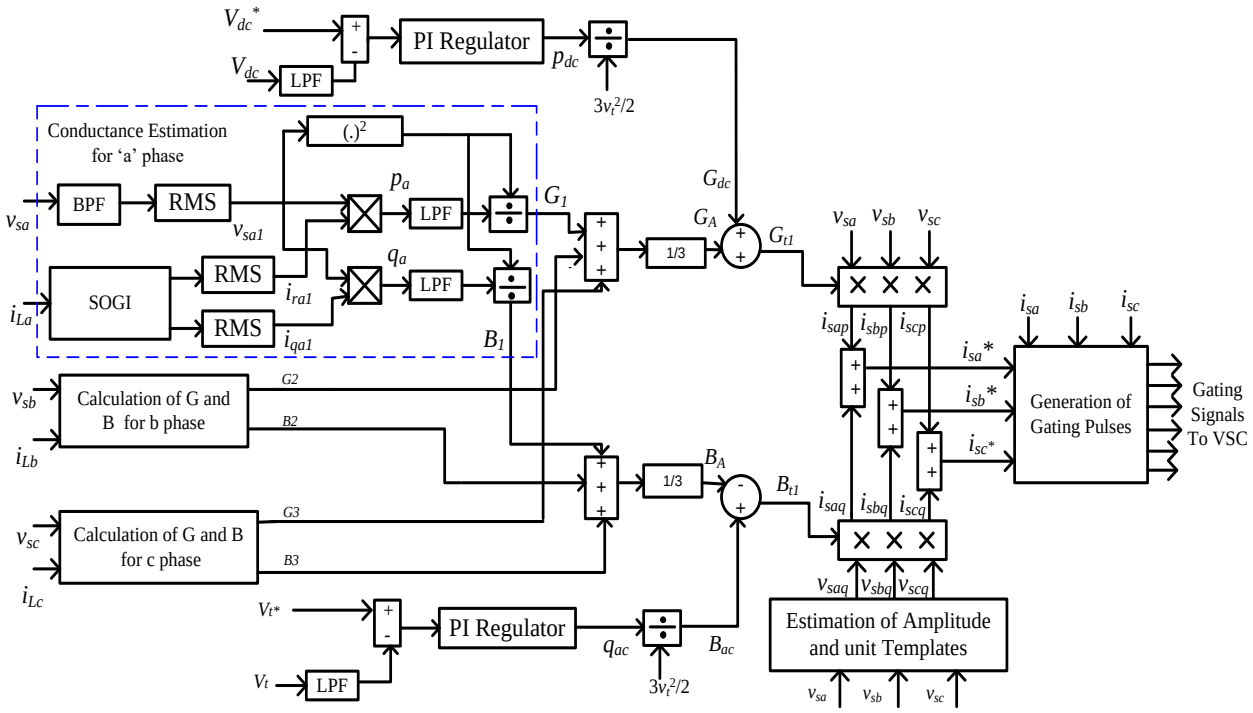


Fig. 2 SOGI based control algorithm for DSTATCOM

In phase Unit templates with phase voltages (w_{pa},w_{pb},w_{pc}) are calculated as,

$$w_{pa} = \frac{v_{sa}}{v_t}, w_{pb} = \frac{v_{sb}}{v_t}, w_{pc} = \frac{v_{sc}}{v_t} \quad (5)$$

Similarly, the quadrature unit templates (w_{qa},w_{qb},w_{qc}) are calculated as,

$$w_{qa} = \frac{(-w_{pb} - w_{pc})}{\sqrt{3}}, w_{qb} = \frac{(3w_{pa} + w_{pb} - w_{pc})}{2\sqrt{3}}, \quad w_{qc} = \frac{(-3w_{pa} + w_{pb} - w_{pc})}{v_t} \quad (6)$$

Quadrature components of PCC voltages are calculated as,

$$v_{saq} = v_t w_{qa}, v_{sbq} = v_t w_{qb}, v_{scq} = v_t w_{qc} \quad (7)$$

C. Estimation of Average Conductance (G_A), Susceptance (B_A) and *Reference Supply Currents*

The sensed PCC phase voltages (v_{sa},v_{sb},v_{sc}) are passed through band pass filter and these values are calculated as (v_{sa1},v_{sb1},v_{sc1}). The load current contains undesirable components like fundamental reactive component, harmonics and DC component along with the fundamental active component because of nonlinear loading. It is desired that source should supply only fundamental component of active current and rest of the components should be compensated by DSTATCOM. A second order generalized integrator is used for the extraction of active and reactive components of the three phase load current. The fundamental active and reactive components of load currents are represented as i_r and i_q respectively. The Fundamental active and reactive power are calculated as,

$$p_a = v_{sa1} i_{ra1}, q_a = v_{sa1} i_{qa1} \quad (8)$$

Similarly it can be calculated for phase B and C as,

$$p_b = v_{sb1} i_{rb1}, q_b = v_{sb1} i_{qb1} \quad (9)$$

$$p_c = v_{sc1} i_{rc1}, q_c = v_{sc1} i_{qc1} \quad (10)$$

The value of the conductances and susceptances observed from PCC are calculated as,

$$G_1 = \frac{p_a}{v_{sa}^2}, B_1 = \frac{q_a}{v_{sa}^2} \quad (11)$$

$$G_2 = \frac{p_b}{v_{sb}^2}, B_2 = \frac{q_b}{v_{sb}^2} \quad (12)$$

$$G_3 = \frac{p_c}{v_{sc}^2}, B_3 = \frac{q_c}{v_{sc}^2} \quad (13)$$

The average amplitude of conductances (G_A) and susceptances (B_A) are calculated as [19],

$$G_A = \frac{G_1 + G_2 + G_3}{3} \text{ and } B_A = \frac{B_1 + B_2 + B_3}{3} \quad (14)$$

Averaging is done for load balancing operation under unbalanced loading. The reference DC voltage (V_{dc}^*) is compared with the measured DC bus voltage (V_{dc}) and the error voltage at r^{th} sampling instant is calculated as,

$$v_{de}(r) = v_{dc}^*(r) - v_{dc}(r) \quad (15)$$

The DC link voltage is regulated by using PI controller. The output of PI controller (P_{cd}) at r^{th} sampling instant is expressed as

$$p_{cp}(r) = p_{cp}(r-1) + k_{dp}[v_{de}(r) - v_{de}(r-1)] + k_{di} v_{de}(r) \quad (16)$$

Where $p_{cp}(r)$ is considered as the per phase active current component drawn from ac mains. k_{dp} and k_{di} are the proportional and integral gain constants of DC link PI voltage controller. The conductance corresponding to DC link (G_{dc}) is calculated as,

$$G_{dc} = \frac{2 p_{cp}}{3 v_t^2} \quad (17)$$

Total conductance (G_{t1}) corresponding to the fundamental active power of source is calculated as,

$$G_{t1} = G_A + G_{dc} \quad (18)$$

Similarly in ZVR mode, PCC voltage is regulated by AC bus PI controller. Output of this PI controller (q_{ac}) at r^{th} sampling instant is expressed as,

$$q_{ac}(r) = q_{ac}(r-1) + k_{tp}[v_{te}(r) - v_{te}(r-1)] + k_{ti}v_{te}(r) \quad (19)$$

Where considered as per phase active current component drawn from ac mains. k_{tp} and k_{ti} are the proportional and integral gain constants of AC bus PI controller. Corresponding value of susceptance (B_{ac}) is calculated as,

$$B_{ac} = \frac{2q_{ac}}{3v_t^2} \quad (20)$$

Total susceptance corresponding to the fundamental reactive power of source is calculated as,

$$B_{t1} = B_A + B_{ac} \quad (21)$$

In phase and quadrature components of reference supply current are calculated as,

$$i_{sap} = G_{t1}v_{sa}, i_{sbp} = G_{t1}v_{sb}, i_{scp} = G_{t1}v_{sc}, \quad (22)$$

$$i_{saq} = B_{t1}v_{sa}, i_{sbq} = B_{t1}v_{sb}, i_{scq} = B_{t1}v_{sc}, \quad (23)$$

Total supply reference currents are calculated as,

$$i_{sa}^* = i_{sap} + i_{saq}, i_{sb}^* = i_{sbp} + i_{sbq}, i_{sc}^* = i_{scp} + i_{scq} \quad (24)$$

Sensed supply currents (i_{sa}, i_{sb}, i_{sc}) are compared with reference supply currents (i_{sa}^*, i_{sb}^*, i_{sc}^*) of respective phases and gating signals for six IGBTs are generated

IV. SIMULATION RESULTS AND DISCUSSION

MATLAB environment with simulink and sim power system tool boxes are used for developing model of DSTATCOM connected to three phase with conductance factor based estimation of reference supply currents. The performance of given control algorithm is observed by simulating it in time domain. The given model is simulated in PFC and ZVR mode with non linear load. Three phase diode based rectifier with R-L load is considered as nonlinear load. Data related to simulation is given in the APPENDIX.

A. Performance of the Control Algorithm

Fig. (5) shows the various parameters including PCC phase voltages (v_{pcc}), load currents (i_L), supply currents (i_s), output of DC link voltage controller (G_{dc}), total conductance (G_{t1}), output of ac bus voltage controller (B_{ac}), total susceptance (B_{t1}) and extracted three phase reference supply currents (i_{abc}^*). These waveforms demonstrate the extraction of control variables under varying non linear load in the ZVR mode of operation. At time (t) = 2.6s, phase 'a' load is injected and it results a small dip into DC link voltage. The 'G_{dc}' represents the active power as a loss component VSC as demands from supply to recover the DC link voltage. It is adjustable during load dynamics as shown in Fig. (5).

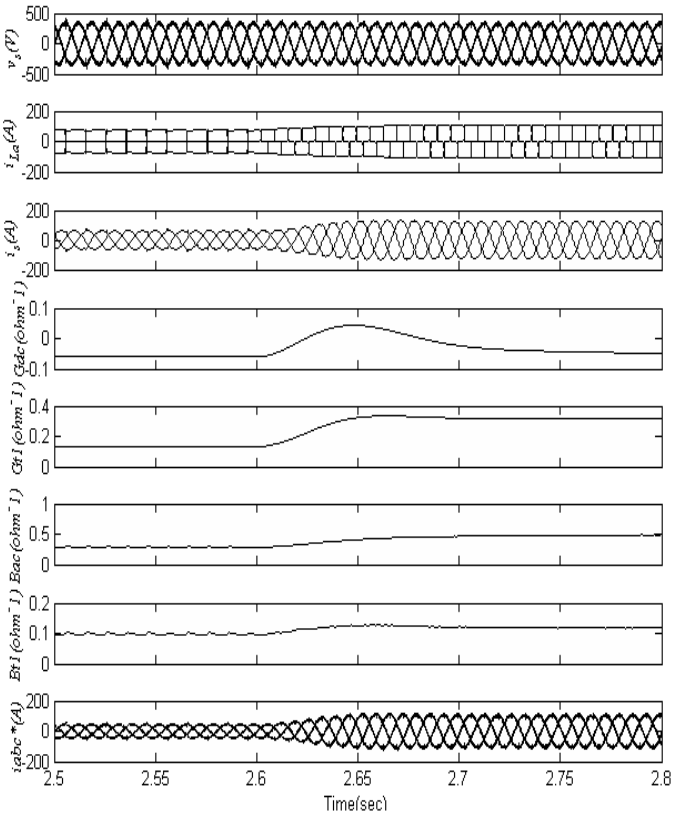


Fig. 5 Variation of internal control parameters under varying nonlinear loads in ZVR mode

B. Performance of DSTATCOM in PFC Mode

The performance of DSTATCOM in PFC mode under varying loading condition is shown in Fig. 6. The performance variables are PCC phase voltages (v_s), supply currents (i_s), load currents (i_{La},i_{Lb},i_{Lc}), shunt currents (i_{fa},i_{fb},i_{fc}) and DC link voltage (V_{dc}) which are shown under load variations (t =2.6s). Before period (t =2.6 s) load is unbalanced but the l supply current remains balanced. At this time, load is connected in phase 'a' which causes momentary dip in DC link voltage. Moreover, it is recovered within some cycles. It is also observed that THD in phase voltages (v_s) and the supply currents are found to be 4.63% and 1.62% respectively where load current THD is 28.31%.

C. *Performance of DSTATCOM in ZVR Mode*

In ZVR mode, DSTATCOM regulates the PCC voltage by injecting extra leading reactive power through the local loop. It is desired to regulating PCC voltage under dynamic loading conditions. Fig. 8, shows dynamic performance of DSTATCOM which is regulating the PCC voltage. After inserting the load at t = 2.6s, DC link voltage is recovered within some cycles. Another side, The PCC voltage is regulated between 325V to 335.5V. In ZVR mode, apart from voltage regulation DSTATCOM also eliminates the harmonics and balances load which can be observed from Fig. 8. In both mode of operation, the voltage and current THD are within 5% as per the guidelines of IEEE standard 519.

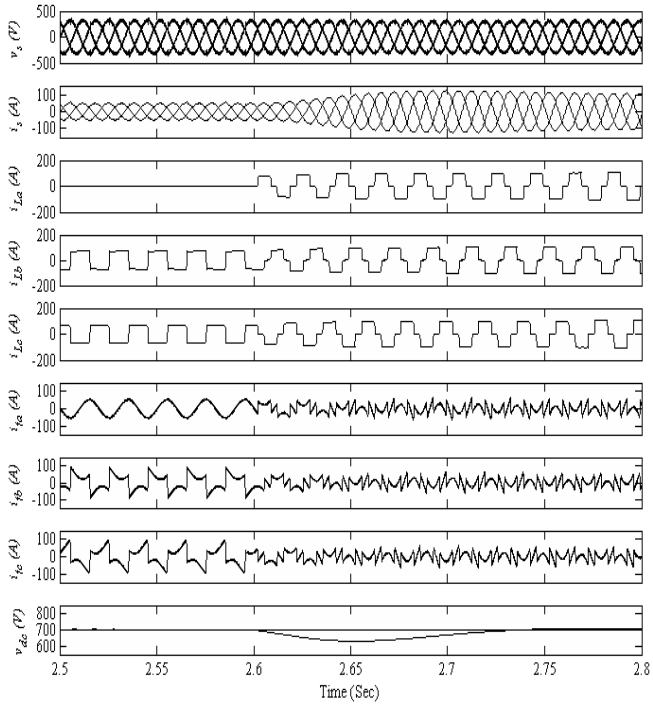
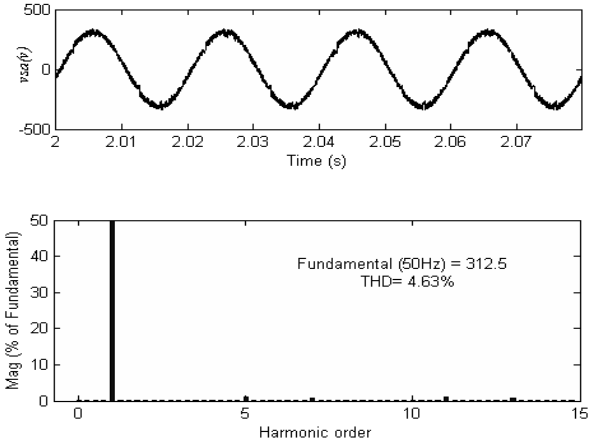
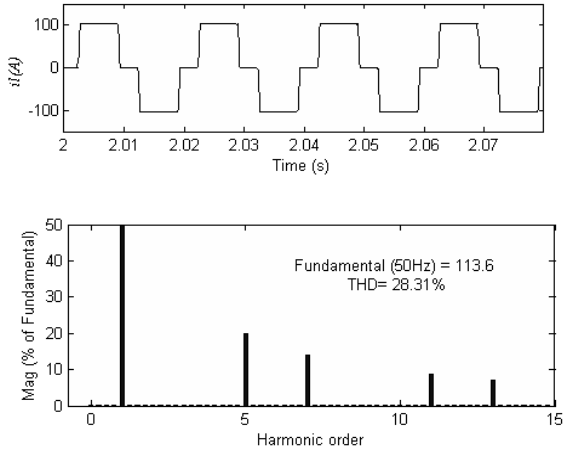


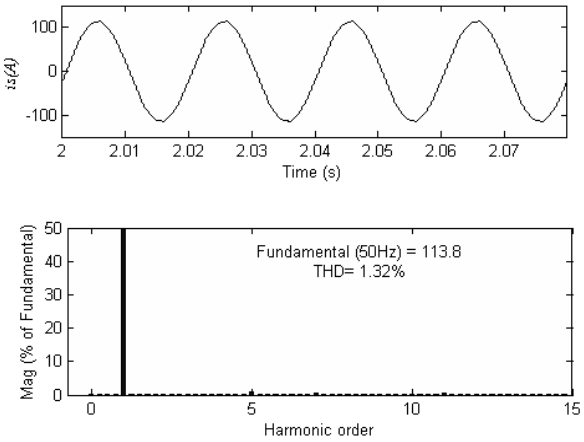
Fig.6 Performance of DSTATCOM in PFC mode



(a)



(b)



(c)

Fig. 7 Waveform Distortion (THDs) (a) PCC phase voltage (b) Load current (c) Supply current.

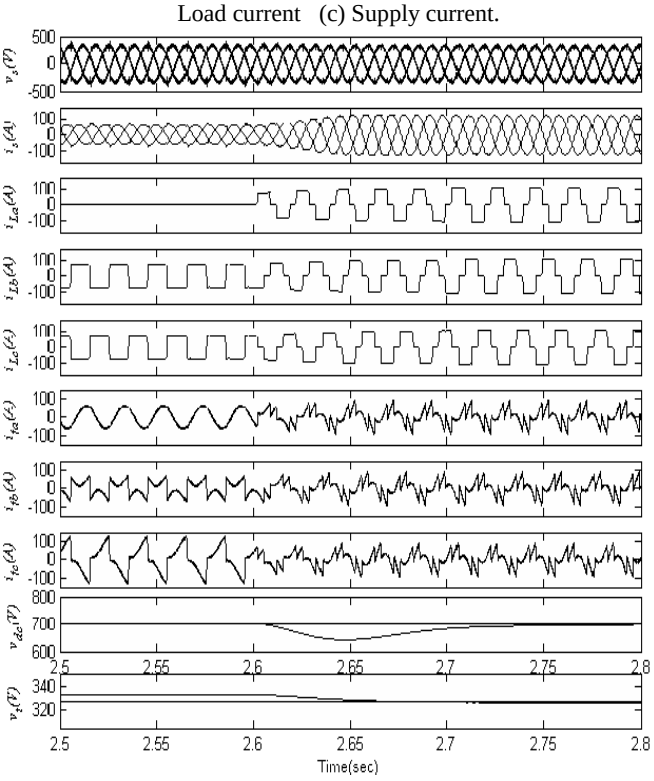
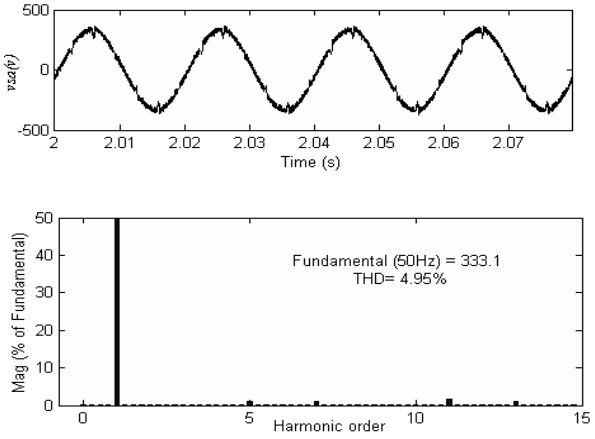


Fig 8 Performance of DSTATCOM in ZVR mode.



(a)

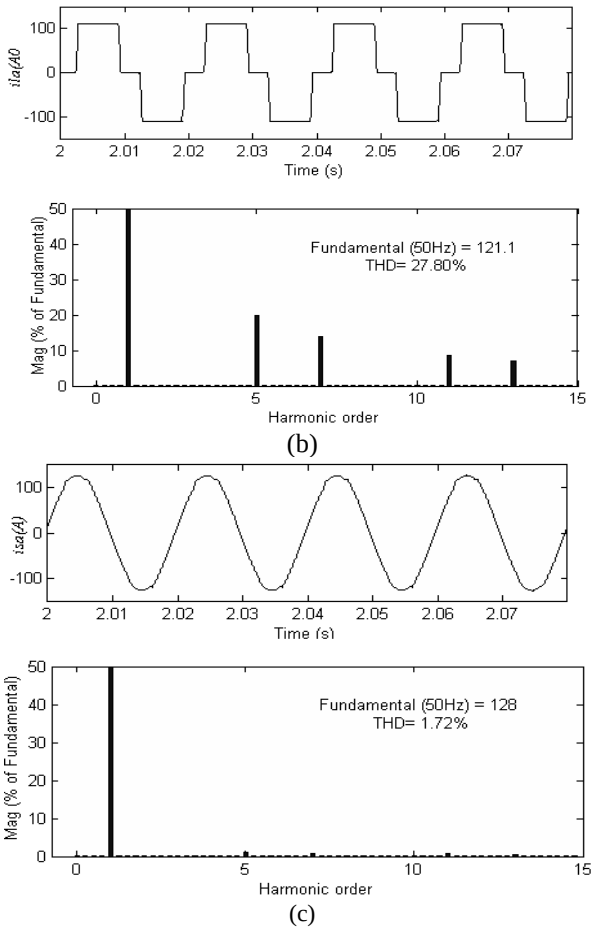


Fig 9. Waveform Distortion (THDs) (a) PCC phase voltage (b) Load current (c) Supply current.

V. CONCLUSION

Three phase DSTATCOM has been simulated after the estimation of load physical parameters through SOGI under nonlinear loads. The performances are obtained by the conductance and susceptance estimation of the load circuit. After application of band pass filter, this algorithm can also able to extract desired supply reference currents under distorted voltage conditions. Some functions of DSTATCOM such as harmonic elimination and load balancing are verified in PFC and ZVR mode under time varying nonlinear load. Source voltage and current are satisfying guidelines of IEEE Std.519-1992 with regulated DC and AC bus voltage. The structure of this algorithm is simple and does not involve any complex calculations or stability issues.

APPENDIX

AC supply: Three phase, 400 V(L-L), 50 Hz; source impedance: R_s=0.08Ω, L_s=1.8 mH; Load-three phase diode rectifier with RL load (current fed type): 5Ω, L=200mH; Ripple filter: R_f=6 Ω,C_f=10μf; DC bus capacitance (C_{dc}) =8000 μf; Reference DC bus voltage (V_{dc}) =700V; Interfacing inductors (L_f) =2mH; DC bus PI controller k_{dp} = 0.4 ,k_{di} = 0.35 ; PCC voltage PI controller k_{pt} =7.2, k_{it} =5.5, Frequency band for band pass filter = 30-70Hz, Cut off frequency of low pass filter = 10 Hz.

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BIOGRAPHIES

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Efficiency Improvement in VSI-fed SPMSM Drive

Chandan Dutta [1] S. M. Tripathi [2]

Abstract–A model-based loss minimization control strategy is presented which reduces the total power loss in a surface-mounted permanent magnet synchronous motor (SPMSM) drive without reducing its dynamic performance. A modified dynamic model of SPMSM (incorporating core loss resistance) is considered. The *d*-axis armature current is utilized to reduce the total power loss in a closed-loop field oriented controlled SPMSM drive. It is found through detailed computer simulations that efficiency of the drive is improved with model-based loss minimization algorithm as compared to the conventional zero *d*-axis current control strategy.

Keywords–Efficiency improvement, field-oriented control (FOC), surface-mounted permanent magnet synchronous motor (SPMSM), loss minimization algorithm (LMA).

NOMENCLATURE

i_d , i_q	*d-q* axes stator current components
i_{cd} , i_{cq}	*d-q* axes iron loss current components
i_{od} , i_{oq}	*d-q* axes magnetizing current components
v_d , v_q	*d-q* axes stator voltage components
L_d , L_q	*d-q* axes stator winding inductances
R_s , R_c	Stator winding and iron loss resistances
ω_e	Angular electrical frequency
ω_m	Rotor mechanical speed
J	Moment of inertia
T_e	Electromagnetic torque
T_m	Load torque
Ψ	Flux linkage due to rotor magnets
Θ	Rotor electrical position
P	Number of pole pairs
F	Damping coefficient
W_{cu}	Stator winding copper losses
W_{fe}	Iron losses
P_{in}	Input power
P_{out}	Output power
W	Total power losses
η	Efficiency

I. INTRODUCTION

Roughly 58% of the total absorbed electrical energy is used in electric motors. Therefore, minimizing the losses and hence efficiency optimization is an important concern in the industry [1–3].

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The widely utilized induction motors exhibit poor efficiency due to copper losses in the rotor circuit [4–6]. Therefore, nowadays permanent magnet synchronous motors (PMSM) are used in variable-speed drive systems due to its high torque-inertia ratio, high power factor, low maintenance cost and robustness.

The motor losses consist of copper losses, iron losses and mechanical losses. Copper losses and iron losses are controllable whereas mechanical losses depend on speed and are not controllable. Copper losses can be reduced by maximum torque-per ampere control (MTPA) and iron losses can be minimized by flux-weakening control [7–8]. Several control techniques have been proposed for loss minimization and efficiency enhancement. Zhou *et al.* [9] increased the efficiency of PMSM drive by incorporating MTPA with fuzzy logic for searching the optimum point. Solutions for MTPA equations were obtained by Newton's method. Lee *et al.* [10] applied Lagrangian to the loss function and numerical techniques were used to obtain the solutions of the fourth order polynomial formed. Also a look-up table was used in the current control loop which was obtained by loss minimizing current sets for given torque and speed. Cho *et al.* [11] used precise parameter estimation for maximizing efficiency of IPMSM drive. Then current phase angles were utilized to determine maximum efficiency point.

In this paper, a control method is presented which reduces the total controllable losses (both iron and copper losses) through the insertion of most optimal *d*-axis current. The results obtained are compared to those obtained with conventional zero *d*-axis current control strategy for a field-oriented controlled SPMSM drive.

II. MODELING EQUATIONS

Conventional PMSM models found in literature do not take iron losses into account. Therefore, in order to obtain a more realistic model, an iron loss resistance R_c aimed for accounting iron losses is inserted in parallel to the magnetizing branch [12–15]. The *d-q* axes stator current components (i_d, i_q) are thus divided into the iron loss current components (i_{cd}, i_{cq}) and magnetizing current components (i_{od}, i_{oq}) as shown in Fig.1.

The steady-state modeling equations of the SPMSM in synchronous reference frame taking into account the iron losses are given by

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = R_s \begin{bmatrix} i_{od} \\ i_{oq} \end{bmatrix} + \left(1 + \frac{R_s}{R_c}\right) \begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} = \begin{bmatrix} 0 & -\omega_e L_d \\ \omega_e L_d & 0 \end{bmatrix} \begin{bmatrix} i_{od} \\ i_{oq} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_e \psi \end{bmatrix} \tag{2}$$

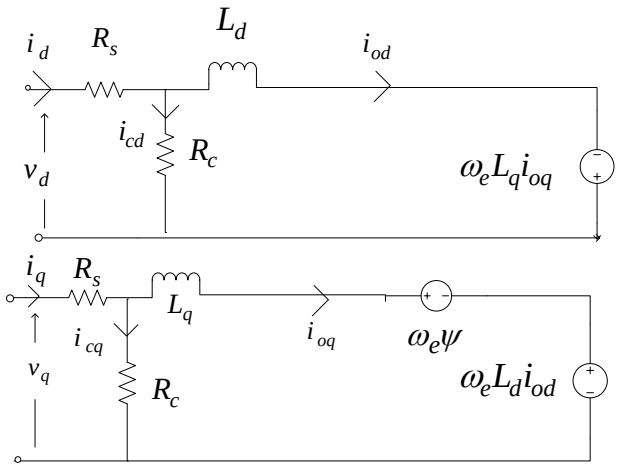

Fig.1. *d-q* axes equivalent circuits for SPMSM model taking iron losses into account under steady-state.

$$i_{cd} = -\frac{\omega_e i_{oq} L_q}{R_c} \quad ; \quad i_{cq} = \frac{\omega_e (\psi + i_{od} L_d)}{R_c} \tag{3}$$

$$i_{od} = i_d - i_{cd} \quad ; \quad i_{oq} = i_q - i_{cq} \tag{4}$$

$$J \frac{d\omega_m}{dt} = T_e - T_m - F\omega_m \tag{5}$$

The electromagnetic torque is given by

$$T_e = 1.5\, P\, [\psi\, i_{oq} + (L_d - L_q) i_{oq}\, i_{od}] \tag{6}$$

For a surface mounted PMSM: $L_d \approx L_q$, so the torque equation becomes

$$T_e = 1.5 P \psi i_{oq} \tag{7}$$

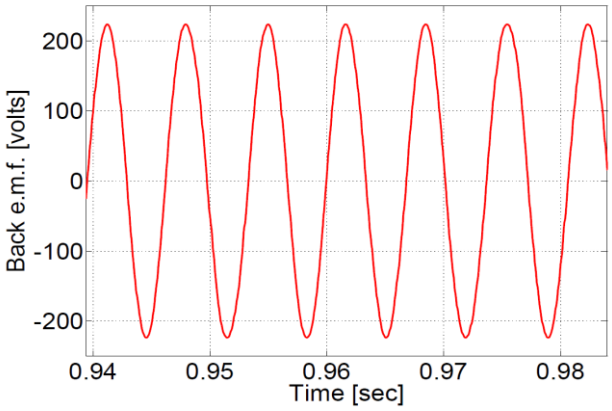

Fig.2. Sinusoidal back e.m.f. waveform of SPMSM.

The back e.m.f. waveform of a SPMSM is induced by the flux coupled with the stator winding and depends on the distribution of the stator winding. The SPMSM block in motoring mode with a closed-loop control system is modeled in MATLAB / Simulink platform which assumes that the stator winding is distributed in a manner that the flux established by the permanent magnets in the stator is sinusoidal and hence, induction of the sinusoidal back e.m.f. as can be seen in Fig.2.

III. Field-Oriented Controlled SPMSM Drive

The proposed schematic is shown in Fig.3. Practically, the actual rotor speed of the SPMSM is measured using a shaft encoder or a resolver and is then compared with the reference rotor speed. The speed error is passed through a speed PI controller to generate the reference stator *q*-axis current. Reference stator *d*-axis current is first set to zero and secondly, it is obtained through model-based loss minimization algorithm. Using inverse Park's transformation, the reference stator *d-q* axes currents are transformed into reference stator *a-b-c* currents. The errors between reference stator *a-b-c* currents and actual stator *a-b-c* currents are regulated through the hysteresis current controllers so as to generate the control signals for the voltage source inverter (VSI) feeding the SPMSM.

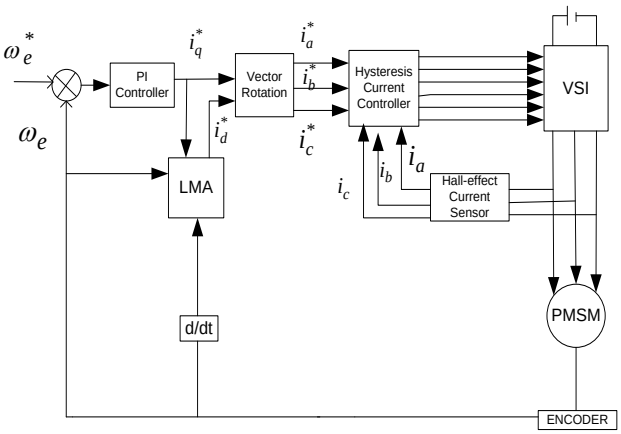

Fig.3. Block-diagram of proposed LMA based SPMSM drive

The values of K_p and K_i are chosen as per the symmetric optimum PI tuning criterion (thoroughly discussed in [16]) and are listed in Appendix.

IV. Model-Based Loss Minimization Algorithm

Based on (1)–(4), the controllable copper losses can be expressed as

$$W_{cu} = \frac{3}{2} R_s \left(i_d^2 + i_q^2\right) \tag{8}$$

$$W_{cu} = \frac{3}{2}\left\{\left(i_{od} - \frac{\omega_e L_q i_{oq}}{R_c}\right)^2 + \left(i_{oq} + \frac{\omega_e (\psi + i_{od} L_d)}{R_c}\right)^2\right\} \tag{9}$$

$$W_{fe} = \frac{3}{2} R_c \left(i_{cd}^2 + i_{cq}^2\right) \tag{10}$$

$$W_{fe} = \frac{3}{2}\left\{\frac{(\omega_e L_q i_{oq})^2}{R_c} + \frac{(\omega_e \psi + \omega_e i_{od} L_d)^2}{R_c}\right\} \tag{11}$$

The total electrical losses are

$$W(i_{od}, i_{oq}, \omega_e) = W_{cu}(i_{od}, i_{oq}, \omega_e) + W_{fe}(i_{od}, i_{oq}, \omega_e) \tag{12}$$

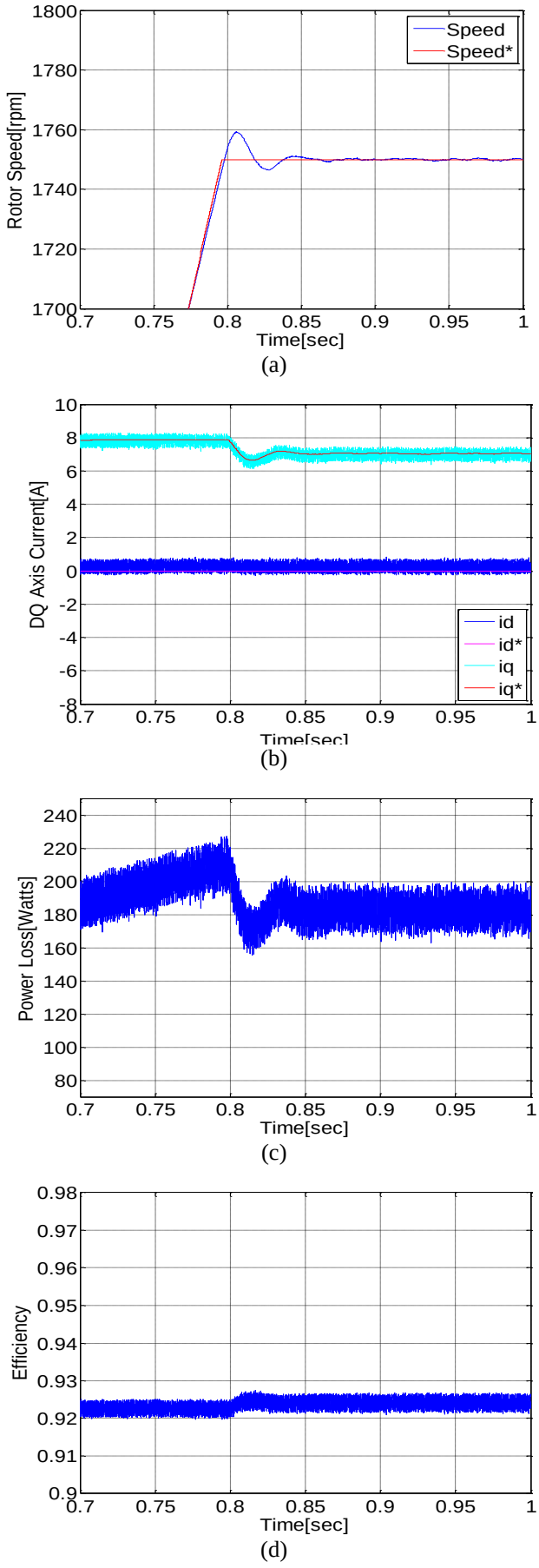

Fig.4. Different responses when rotor accelerates from 0 to 1750 rpm at constant load torque of 12 N-m with conventional i_d = 0 approach—(a) rotor speed (b) stator *d-q* axes currents (c) Power loss (d) efficiency.

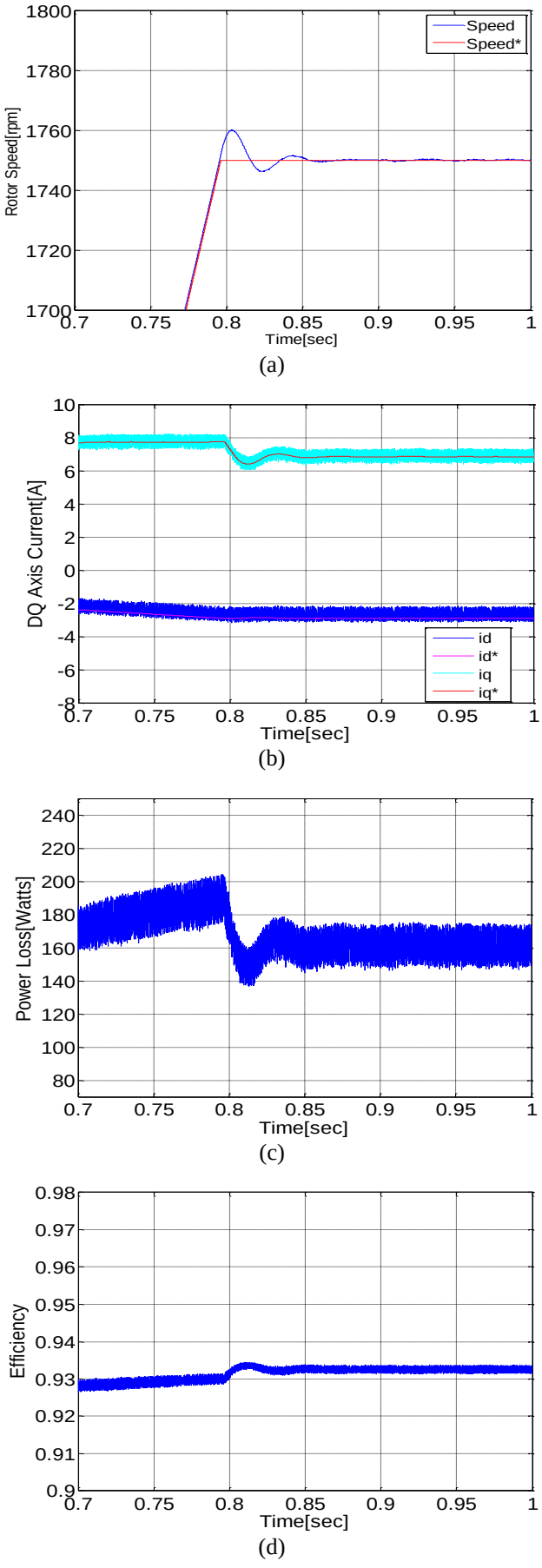

Fig.5. Different responses when rotor accelerates from 0 to 1750 rpm at constant load torque of 12 N-m with proposed model-based LMA—(a) rotor speed (b) stator *d-q* axes currents (c) Power loss (d) efficiency.

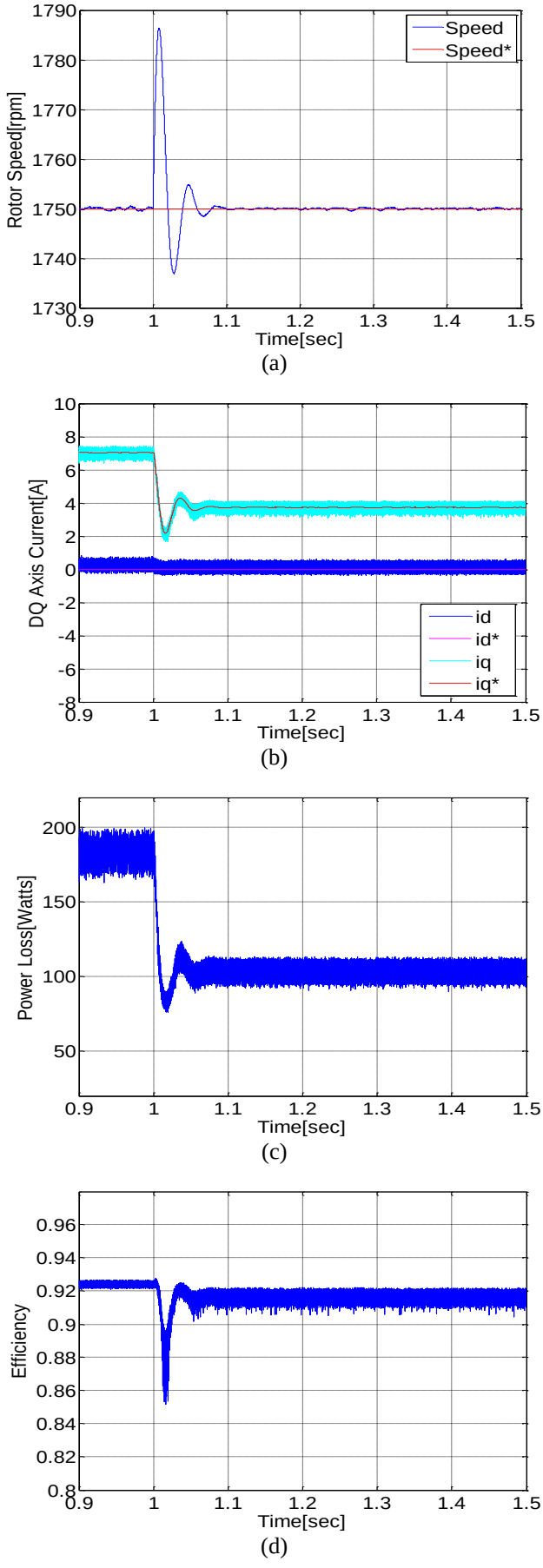

Fig.6. Different responses when load torque is reduced from 12 to 6 N-m at constant rotor speed of 1750 rpm with conventional i_d = 0 approach—(a) rotor speed (b) stator *d*-*q* axes currents (c) Power loss (d) efficiency.

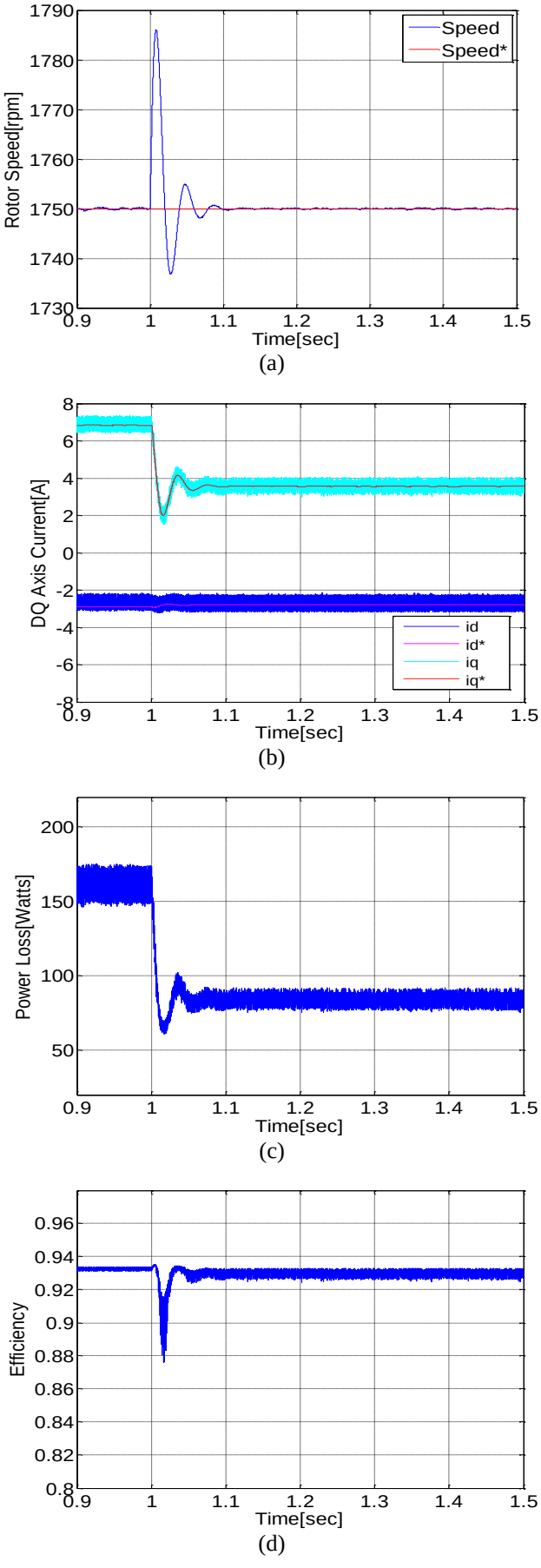

Fig.7. Different responses when load torque is reduced from 12 to 6 N-m at constant rotor speed of 1750 rpm with proposed model-based LMA—(a) rotor speed (b) stator *d*-*q* axes currents (c) Power loss (d) efficiency.

By differentiating (12) with respect to i_{od} and equating it to zero, we get the optimum *d*-axis current for which losses are minimum *i.e.* $\frac{\partial W}{\partial i_{od}} = 0$ (assuming T_e and ω_e constant).

$$i_{od}^{*} = -\frac{\psi L_d \omega_e^{\,2}\left(R_s + R_c\right)}{R_s R_c^{\,2} + \omega_e^{\,2} L_d^{\,2}\left(R_s + R_c\right)} \tag{13}$$

The output power P_{out} and efficiency of the motor η is expressed as follows:

$$P_{out} = \omega_e T_e \tag{14}$$

$$\eta = \frac{P_{out}}{P_{out} + W} \tag{15}$$

V. Performance Comparison

The drive is simulated using MATLAB / Simulink platform. The drive performance for efficiency enhancement is tested for various transient conditions. However, keeping in view the page constraint, only two transient cases *viz.* (a) start-up at rated load and (b) reduction in load torque are included in this paper so as to provide a glimpse of the effectiveness of the proposed approach for efficiency improvement in the SPMSM drive.

At first, the motor is at standstill. A speed command of rated value (1750 rpm) at rated load (12 N-m) is given. The speed of the rotor sets in 0.858 seconds with conventional control approach (i_d = 0) and efficiency is recorded as 92.40%, while 0.854 seconds with model-based LMA and efficiency is recorded as 93.25%. From the curves of Figs. 4–5, it is seen that total loss is minimized and the efficiency is improved.

Table 1: Summary of different transient cases presented

Performance parameters	Conventional i_d=0 approach	Model-based LMA
***Case 1*- Speed: 0 rpm to 1750 rpm at Load Torque: 12 N-m**		
Maximum overshoot (%)	0.510	0.570
Drive settling time (s)	0.858	0.854
Efficiency (%)	92.40	93.25
***Case 2*- Load Torque: 12 N-m to 6 N-m at Speed: 1750 rpm**		
Maximum overshoot (%)	2.070	2.060
Drive settling time (s)	0.098	0.096
Efficiency (%)	91.60	92.95

Further, the load torque on the motor running at 1750 rpm is decreased from 12 N-m to 6 N-m at time t = 1 sec. As a result, the rotor speed tends to increase however, it again settles to 1750 rpm in 0.098 seconds with conventional control approach and efficiency is recorded 91.60% while 0.096 sec. with model-based LMA and efficiency is noted as 92.95%. From the curves of Fig.6 and Fig.7 it is seen that losses are minimized and efficiency is improved for this case also.

From Table–1, it can be seen that the drive settling time and maximum overshoot is nearly the same for both control strategies. From this a conclusion can be made that the dynamic performance of the drive is not affected and still the efficiency is improved.

VI. Conclusions

A model-based LMA scheme for SPMSM drive was presented. The *d*-axis armature current was utilized and optimally controlled for loss minimization and hence maximizing the efficiency. To compare the performance of the drive, field-oriented control strategy, firstly with conventional zero *d*-axis current control and secondly with model-based loss minimization algorithm was adopted. Results of simulation show that the dynamic performance of the drive is not affected and efficiency of the drive is improved with model-based loss minimization algorithm.

Appendix

Parameters of the SPMSM used in simulation model are as follows: Power P_o = 2.2 kW; Number of pole pairs P = 5; J = 0.007 Kg-m^2; R_s = 1.72 Ω; R_c = 700 Ω; ψ = 0.244 Wb; L_d = 20.5 mH; L_q = 20.5 mH; PI Controller parameters: K_p = 0.7876; K_i = 271.5862

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A Simple Control of STATCOM for Non-linear Load Compensation

Prakash Ji Barnawal [1] S. M. Tripathi [2]

Abstract–This paper presents a simple controller for non-linear load compensation by using a three-phase voltage source converter (VSC) based static synchronous compensator (STATCOM). The PI tuning criteria 'modulus optimum (MO)' and 'symmetric optimum (SO)' are used in order to make the system faster, robust and disturbance free. The controller forces the source quadrature current to be zero so that the source supplies only real power to the load. The proposed scheme is simulated in MATLAB environment.

Keywords–DC voltage control, modulus optimum criterion, static synchronous compensator, symmetric optimum criterion, voltage source converter.

NOMENCLATURE

MO	Modulus optimum
PCC	Point of common coupling
SO	Symmetric optimum
VSC	Voltage source converter
V_{LL}	PCC line-line voltage
i_{abc}	Three-phase source current
V_{dc}	DC capacitor voltage
L	AC inductor
R	Resistance of AC inductor
K_{pi}	Proportional gain of current PI controller
K_i	Integral gain of current PI controller
T_i	Integral time constant of current PI controller
K_{po}	Proportional gain of DC voltage PI controller
K_{io}	Integral gain of DC voltage PI controller
T_o	Integral time constant of DC voltage PI controller

I. INTRODUCTION

The power quality has always been a matter of concern for any electrical distribution system. It involves the consideration not only from the source side but also from the load side. Since last few decades, the use of power electronic interfaces has been increased to a great extent that allows the consumer to use the power in the required way. The use of such interfaces distorts the system waveforms and causes a poor power quality. The IEEE 100 (authoritative dictionary of IEEE standard terms) acknowledges the definition of the power quality [1]. IEEE 519-1992 standards prescribe the power practices and requirements for limiting the harmonics in the power system [2].

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Reactive power arises due to the energy storing elements *viz*. inductor and capacitor in the electrical network and refers to the portion of power which does not contribute to the energy conversion / transformation but circulates back and forth in each cycle in the power system [3–4]. It is primarily responsible for maintaining the voltages for the normal operation of the electrical power system and is required for the magnetization of the electric machines as well [5]. With the reactive load connected in the electrical network the power factor becomes worsen. As a consequence, the reactive power demanded by the load from the source should be kept a minimum.

It is possible to improve the power factor by means of a compensator which generates the reactive power equal and opposite to the load reactive power and does not affect the active power of the load. Active compensators based on the custom power devices are nowadays common in industry applications for both reactive power compensation (power factor correction) as well as harmonic mitigation. However, the reactive power compensation should be provided as close as possible to the consumer / load point.

The STATCOM is the second generation shunt connected FACTS device that works as a static VAR compensator. The choice of STATCOM lies behind its property of faster and better transient / dynamic responses, and enhanced capability to exchange power [6]. However, the proper working of the STATCOM is dependent on the switching signals generated by its controller [7]. This paper basically focuses on the design of a controller for STATCOM.

Many literatures [7–12] have already proposed the designing of controller for STATCOM. Singh *et al.* [7] presented control algorithm based on correlation and cross correlation function approach for power quality improvement. Schauder *et al.* [8] presented two advanced static VAR compensator inverter for control of the output voltage magnitude and phase angle. Chen *et al.* [9] presented a novel STATCOM controller with a fixed modulation index reference to minimize the voltage and current harmonics. Cheng *et al.* [10] presented an integrated model of energy storage system and STATCOM. Escobar *et al.* [11] presented a passivity-based controller for a STATCOM for the compensation of reactive power and harmonics. Ledwich *et al.* [12] presented a paper where a discussion on voltage and current control of STATCOM is given.

In this paper, a brief description of the STATCOM system and its control scheme is discussed. The control scheme is developed such that the controller forces the source current to be sinusoidal. The performance results of the control scheme are shown with the help of the harmonic spectra and waveforms.

II. System Description and Proposed Controller Scheme

The configuration of the system is represented as shown in Fig.1. An AC supply is acting as a source of magnitude *V* and frequency *f*. Here, the STATCOM is represented as a three-phase VSC empowered by a large DC capacitor.

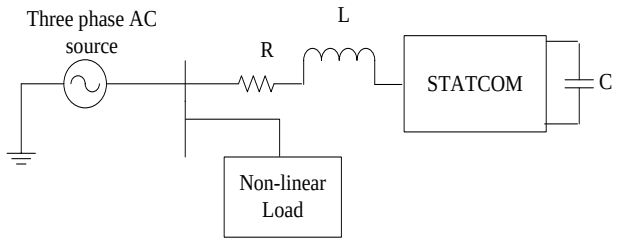

Fig.1. The configuration of the proposed system.

The proposed control schematic for the STATCOM is illustrated in Fig.2. The objective of the controller is to generate the switching pulses in such a way so that it could compensate the non-linear load and force the source currents to be sinusoidal. It is achieved by voltage oriented control wherein two loops (*viz*. inner current control loop and outer DC voltage control loop are involved) and the source quadrature component is forced to be zero so that only real power is supplied by the source to the non-linear load.

For the conversion from the *a-b-c* reference frame to synchronously rotating *d-q* reference frame, two transformations are required. Clark's transformation is used to convert three-phase AC quantities from *a-b-c* reference frame into *α-β* reference frame and Park's transformation is applied for converting *α-β* reference frame into *d-q* reference frame. The reason behind choosing *d-q* reference frame is its ability to decouple both the real and reactive powers and making them independent of each other.

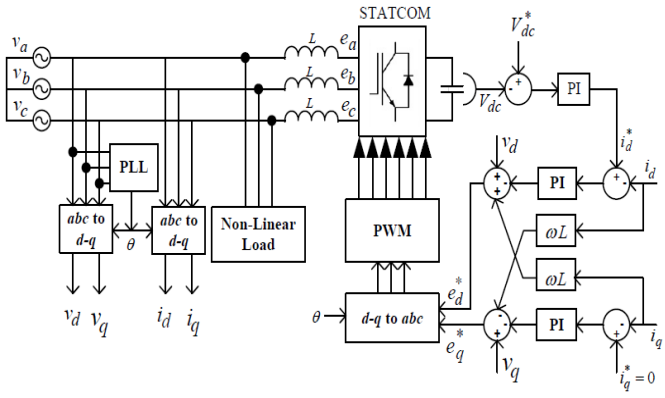

Fig.2. Proposed control schematic for STATCOM.

The involved PI controllers can be tuned by means of different tuning methods. However, tuning of the PI controller parameters is always a challenging job to engineers because of uncertain plant. Every tuning method has its own constraints and limitations as thoroughly discussed in [13]. The 'modulus optimum (MO)' and 'symmetric optimum (SO)' criteria are identified as one of the straightforward optimum PI tuning criteria offering satisfactory set-point response of the closed-loop system without requiring complete plant model [13–14]. In order to make the inner current control loop work faster and oscillation free, the tuning of the inner loop current PI controller is carried out with the MO criterion wherein, the dominant pole of the plant is cancelled with the controller zero. On the other hand, the tuning of the outer-loop DC voltage PI controller is carried out with the SO criterion [15] in order to achieve optimum regulation and system stability along with better rejection to the disturbance and maximized phase margin. A modus operandi is presented in the upcoming sub-sections so as to calculate the PI controller gains for the inner current as well as outer DC voltage control loops.

A. Current control loop

The block-diagram of the current control loop is shown in Fig.3. The PWM converter acts as a transformer with a time-lag converting the reference voltage to a different voltage level. The average time-lag T_w for the control delay and PWM converter blocks as shown in Fig.3 is 1.5 times the sampling time T_{sample} of the current control loop [13].

$$T_w = 1.5\ T_{sample} \tag{1}$$

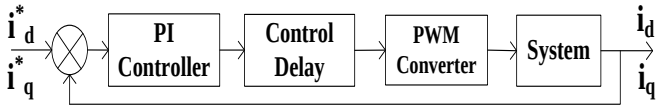

Fig.3. Block-diagram of the inner current control loop.

The open-loop transfer function for the current control loop is given as

$$G_{C,OL}(s) = \frac{i_d}{i_d^*} = \frac{i_q}{i_q^*} = K_{pi}.\left(\frac{1+T_i s}{T_i s}\right).\left(\frac{1}{1+T_w s}\right).\frac{1}{R}.\left(\frac{1}{1+\tau s}\right) \tag{2}$$

where, $T_i = (K_{pi}/K_i)$ and $\tau = L/R$.

In order to make the current control loop work faster and oscillation free, tuning of the PI controller is carried out with MO criterion. After applying the MO tuning criterion, the closed-loop transfer function of the current control loop is found to be as

$$G_{C,CL}(s) = \frac{1}{2T_w^2.s^2 + 2T_w.s + 1} \tag{3}$$

It can easily be deduced from the transfer function mentioned above that the damping ratio is $\xi = 0.707$. The estimated values of the proportional and integral gains of the current PI controller are

$$K_{pi} = \frac{\tau R}{2T_w} \quad \text{and} \quad T_i = \tau \tag{4}$$

B. DC voltage control loop

The block-diagram of the DC voltage control loop is shown in Fig.4. The open-loop transfer function of the outer control loop may be given as

$$G_{O,OL}(s) = \frac{K_{po}.K}{sT}\left(\frac{1+T_0 s}{T_0 s}\right).\left(\frac{1}{1+T_e s}\right) \quad (5)$$

where, $K = v_d / V_{dc}$ and $T = 2C/3$ $T_e = 2T_w + 10T_{sample}$.

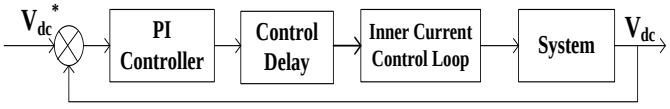

Fig.4. Block-diagram representation of the outer DC voltage control loop.

The tuning of the DC voltage control loop is carried out with SO criterion. After applying the SO tuning criterion, the closed-loop transfer function for the DC voltage control loop is given as

$$G_{O,CL}(s) = \frac{1+a^2.T_e.s}{(a.T_e.s+1)\left(a^2.T_e^2.s^2 + a.(a-1).T_e.s+1\right)} \quad (6)$$

The estimated values of the proportional and integral gains of the DC voltage PI controller are

$$K_{po} = \frac{T}{a.K.T_e} \quad \text{and} \quad T_o = a^2.T_e \quad (7)$$

where, the value of parameter '*a*' may vary from 2 to 4 [13]. The calculated values of the controller parameters are listed in Table–1.

Table.1: System parameters

Parameters	Value	Controller Parameters	Value
V_{LL}	415 V	K_{pi}	26.06
V_{dc}^*	800 V	K_i	12000
R	1.8Ω	K_{po}	2.5829
L	3.91 mH	K_{io}	445.3274

III. Simulation Results

An unbalanced non-linear inductive load is connected at the PCC. The non-linear loads drawing harmonic currents from the AC source result in the distortion in the voltage waveforms at the PCC, the magnitude of which mainly depends on the source impedance [16]. However, in this paper, the stiff AC supply system with negligible (almost zero) impedance is considered between the AC source and the PCC. In simulation model, three single-phase diode bridge rectifiers connected in delta configuration and feeding the impedances of values 12+*j*120*e*-3, 24+*j*12*e*-3 and 36+*j*1.2*e*-3, respectively at the DC side constitute an unbalanced non-linear load connected at the PCC.

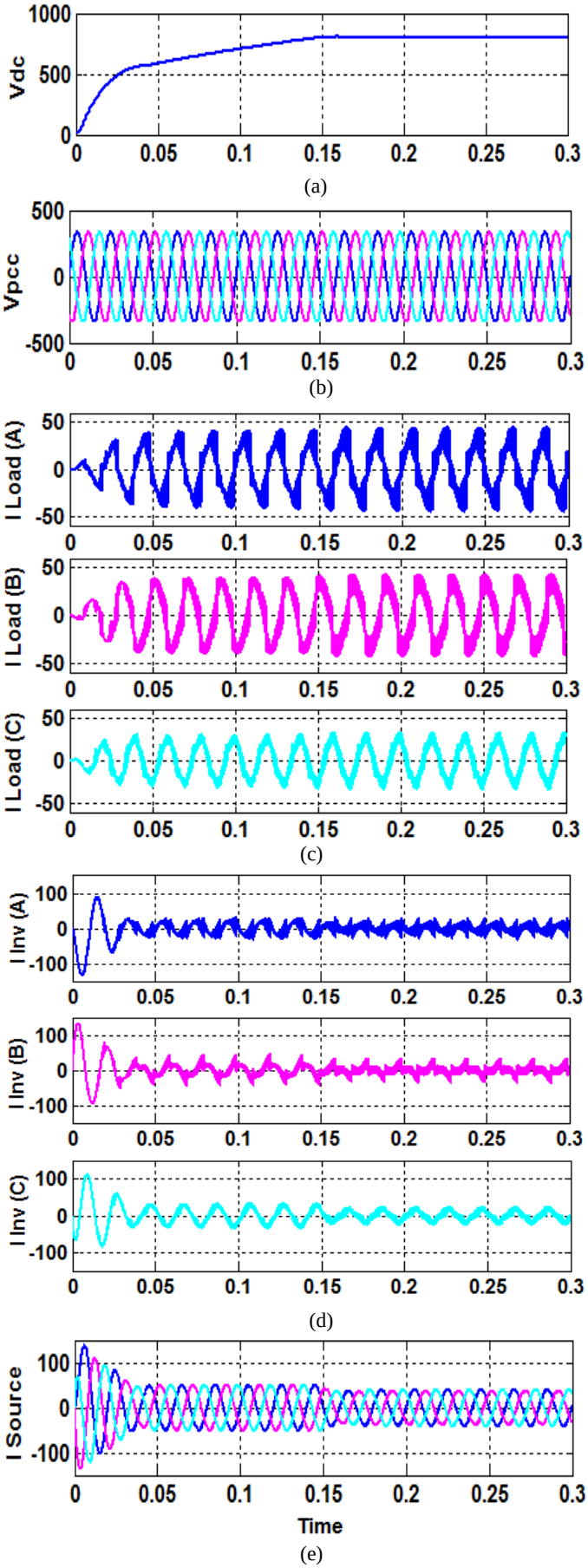

Fig.5. Performance of the proposed STATCOM control—(a) DC capacitor voltage (b) voltages at PCC, (c) load currents for phases *a*, *b* and *c*, respectively (d) inverter (STATCOM) currents for phases *a*, *b* and *c*, respectively (e) source currents.

The waveforms for the different currents and voltages are presented along with current harmonic spectra as shown in Figs. 5–6. From Fig.5 (a) it can be seen that the DC voltage is settled at its reference value of 800 volts. Fig.5 (b) shows the voltages at the PCC which is completely sinusoidal. The load currents profile is shown in Fig.5 (c). The inverter (STATCOM) current compensation is shown in Fig.5 (d) and the three-phase source currents are shown in Fig.5 (e). Further, Fig.6 shows the harmonic spectra of the load and the source currents for all three phases. The THDs of the load and the source currents are listed in Table–2.

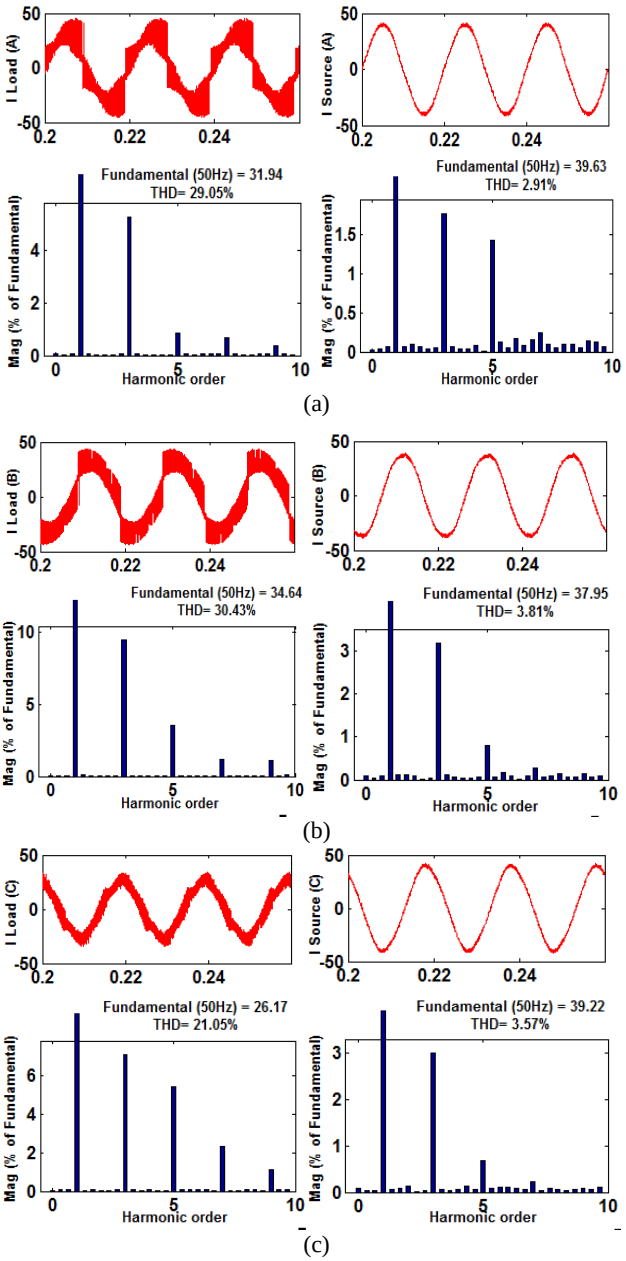

Fig.6. Load and source current waveforms and their harmonic spectra—(a) phase '*a*' (b) phase '*b*' (c) phase '*c*'.

It is worth noticeable that for a standard single-phase bridge rectifier (which is used here in constituting the non-linear load), the number of pulses $p = 2$ in one cycle of the line frequency and, therefore, the characteristic harmonics are $h = 2n \pm 1$ *viz.* 1 (fundamental), 3, 5, 7, 9, 11… *etc.* wherein, the lower order harmonics such as 3rd, 5th and 7th are dominant [17]. This is also apparent in the current harmonic spectra shown in Fig.6. It can be concluded that the STATCOM controller forces the source current to be sinusoidal by compensating the non-linearity in the load-currents. Further, the THDs of the source currents are within 5% as per IEEE-519 standard.

Table.2: THDs of the source and load currents

Phase	Source Current		Load Current	
	Magnitude (A)	THD (%)	Magnitude (A)	THD (%)
a	39.63	2.91	31.94	29.05
b	37.95	3.81	34.64	30.43
c	39.22	3.57	26.17	21.05

IV. Conclusions

A simple control of a three-phase VSC based STATCOM was presented and studied. For obtaining oscillation and delay free response, two different tuning criteria *i.e.* MO and SO were applied. These tuning criteria were found to be responding very well. The voltage and current waveforms corresponding to the case of unbalanced non-linear load were observed and the controller was found functioning well. The THDs of the source currents were found to be under the limit of 5% as per IEEE-519 standard.

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Prakash Ji Barnawal was born in Bhadohi, India in 1991. He completed his B.Tech. degree from Galgotias College of Engineering & Technology, (U.P.), India in the year 2014 and M.Tech. degree in Power Electronics & Drives from Kamla Nehru Institute of Technology, (U.P.) India in the year 2016. His fields of current interest include power quality, power electronics and electric drives.

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